

PC Codec with 2 V_{RMS} -capable Headphone Driver

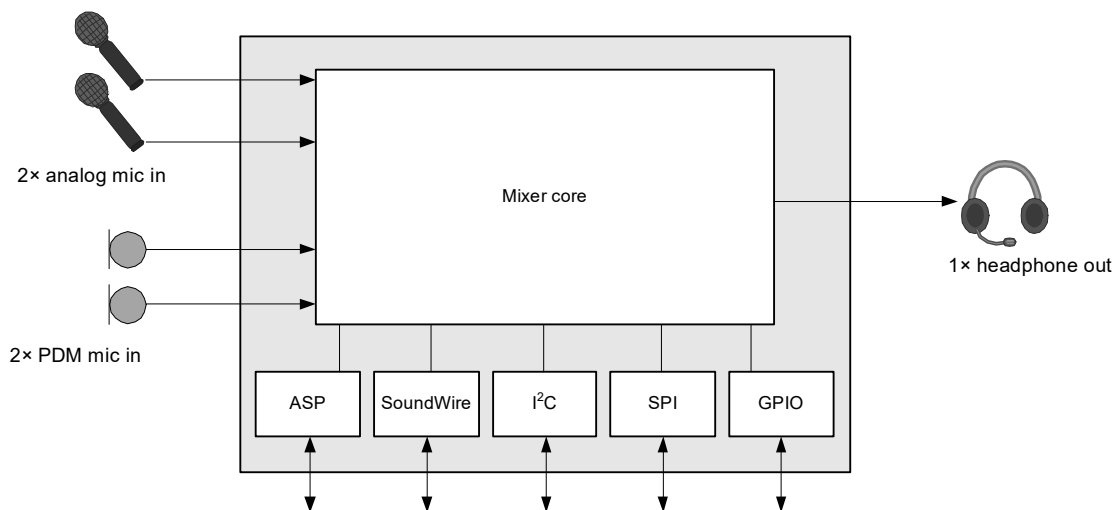
System Features

- Stereo headphone (HP) output with 114 dB dynamic range
 - Class G headphone amplifier with automatic and manual supply configurations
 - -93 dB THD+N into 30 Ω at 10 mW power output
 - 1 V_{RMS} output swing into 30 Ω loads
 - 2 V_{RMS} output swing into 600 Ω loads
 - Load detection
 - Supports sample rates up to 192 kHz
- Stereo mic/line-in input with 94 dB dynamic range
 - Headset bias with integrated bias resistor
 - 2 V_{RMS} input voltage for line-in inputs
 - Programmable analog front end (AFE) gain from -6 to +24 dB in 6 dB steps
- Integrated detect features
 - OMTP (Open Mobile Terminal Platform) and CTIA headset-type detection and configuration with low-impedance internal switches
 - Mic button press detect with ADC automute
 - Mic button detection compatible with Android Wired Headset Specification (Version 1.1)
 - Automatic clamp of headset bias output on headset bias current drop or HP/headset unplug
- System wake from headset/headphone plug/unplug or mic button press
- Stereo three-band parametric equalizers

- I²C control supporting rates up to Fast Mode Plus
- MIPI® SoundWire® v1.2.1 interface with SDCA v1.0 support
- S/PDIF transmit (Sony/Philips digital interface format)
- Integrated fractional-N PLL
 - Allows multiple clock input rates
 - Reference clock sourced from either SoundWire clock or external MCLK_IN source
- PDM input for digital microphones
 - Supports output decimation rate up to 96 kHz
- Audio serial port (ASP)
 - I²S (two channels) or TDM (up to eight channels)
 - Controller or Target Mode
 - Sample rate support for 8 to 192 kHz
- Integrated power management
 - Digital core supplied by internal LDO from VDD_A supply
 - Class G headphone amplifier improves HP efficiency

Applications

- Laptops
- Desktops
- Ultrabooks
- Chromebooks
- Portable audio devices



General Description

The CS42L45 is an audio codec with integrated MIPI SoundWire interface (Version 1.2.1 compliant) with SDCA v1.0 support, I²C, and I²S/TDM interfaces designed for portable applications. It provides a high dynamic range, stereo DAC for headphone output, and two ADCs for wired headset microphone input or stereo line input. PDM inputs are provided to support up to four digital microphones. Each digital microphone path supports three volume controls. All four digital microphone paths and both ADC paths are available simultaneously.

The CS42L45 provides high performance audio capture from the ADC and PDM inputs and audio playback to the headphone DACs, and an IEC-60958-3-compatible S/PDIF transmitter. The CS42L45 includes assignable sample rate converters (SRCs) and an assignable stereo, three-band, 32-bit, parametric equalizer.

Digital mixers are available with independent attenuation on each mixer input.

Digital volume/mute control is available on all capture and playback paths and selectable high-pass filters are available on the capture paths for removal of DC offsets and wind noise suppression.

A headset mic bias with an integrated pull-up resistor is provided for use with the headset interface. Other headset features include automatic headset type detection (OMTP/CTIA-compliant), mic-bias/ground switching, and headset-button detection including Android Wired Headset Specification v1.1. Other features include insert/removal detection, headphone load impedance detection, and stereo line-in support.

A high performance fractional PLL is available for generating internal audio sample clocks.

The CS42L45 is available in a commercial-grade, 42-ball WLCSP (wafer-level chip scale package) for operation between -40°C and +85°C. Note that the WLCSP package can be routed using a standard PCB with vias.

See [Section 5](#) for ordering information.

1 Pin Assignments and Descriptions

1.1 WLCSP Pin Out (Through-Package, Top View)

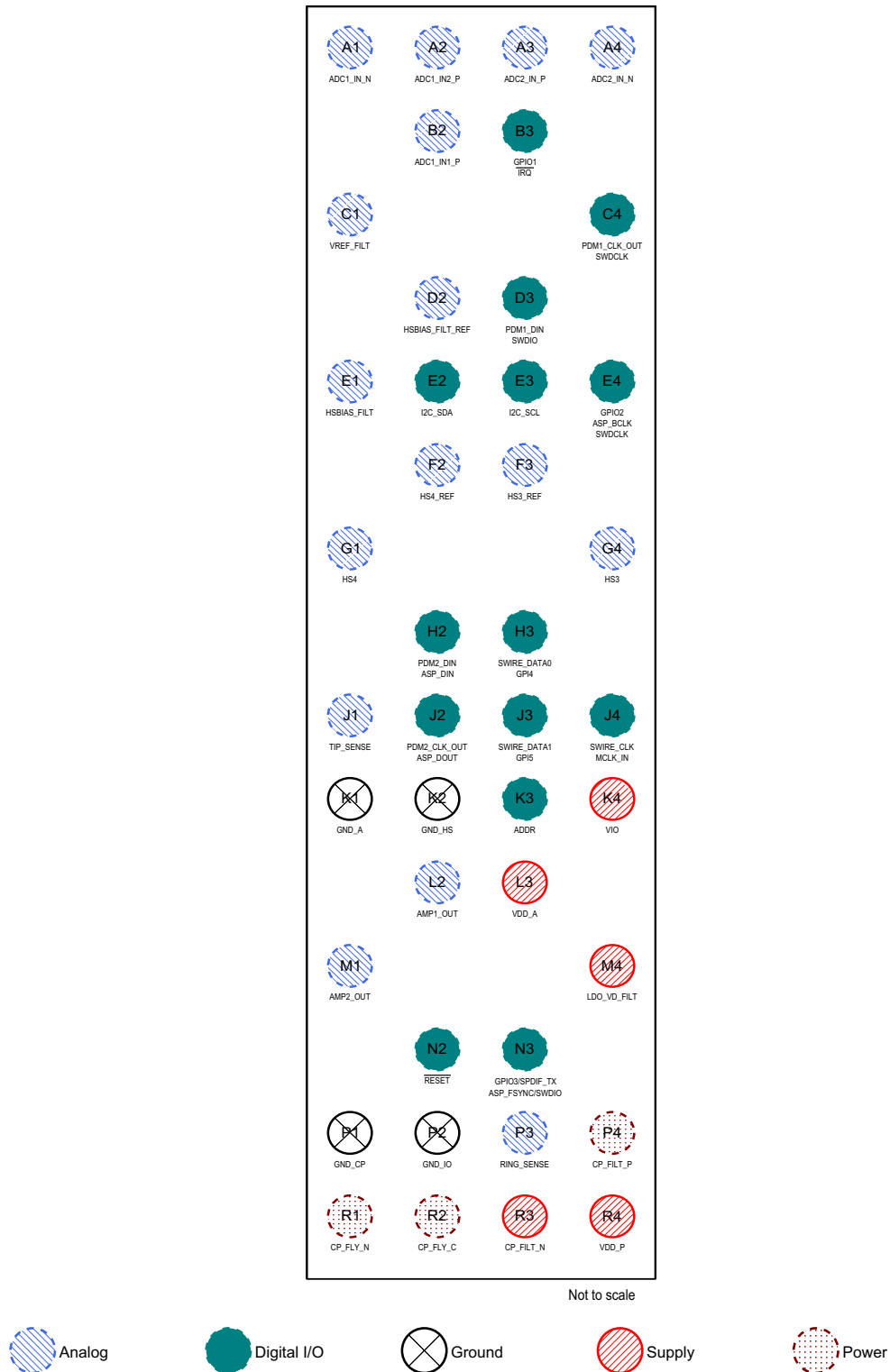


Figure 1-1. WLCSP Ball Diagram (Through-Package, Top View)

1.2 WLCSP Pin Descriptions

Table 1-1. WLCSP Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
ADC1_IN1_P	B2	VDD_P	I	Non-inverting analog input for ADC 1 mux input 1.	—	—
ADC1_IN2_P	A2	VDD_P	I	Non-inverting analog input for ADC 1 mux input 2.	—	—
ADC1_IN_N	A1	VDD_P	I	Inverting analog input for ADC 1.	—	—
ADC2_IN_N	A4	VDD_P	I	Inverting analog input for ADC 2.	—	—
ADC2_IN_P	A3	VDD_P	I	Non-inverting analog input for ADC 2.	—	—
ADDR	K3	VIO	I	Address select for I2C and SoundWire. Connect this pin to VIO or GND.	Weak pull down	Weak pull down
AMP1_OUT	L2	CP_FILT_P/ N	O	Amplifier 1 Output. Ground-centered audio output typically used for headphone speakers and connects to TIP (HS1).	—	—
AMP2_OUT	M1	CP_FILT_P/ N	O	Amplifier 2 Output. Ground-centered audio output typically used for headphone speakers and connects to RING1 (HS2).	—	—
CP_FILT_N	R3	Power	O	Inverting Charge Pump Filter Connection. Power supply for the inverting charge pump that provides the negative rail for amplifiers 1 and 2.	—	—
CP_FILT_P	P4	Power	O	Non-Inverting Charge Pump Filter Connection. Power supply for the step-up/down charge pump that provides the positive rail for amplifiers 1 and 2.	—	—
CP_FLY_C	R2	VDD_P	O	Charge Pump Cap Common Node. Common node for amplifiers 1 and 2 charge-pump flying capacitor.	—	—
CP_FLY_N	R1	CP_FILT_P	O	Charge Pump Cap Negative Node. Negative node for amplifiers 1 and 2 charge-pump flying capacitor.	—	—
GND_A	K1	Power	I	Analog Ground. Ground reference for the internal analog circuits.	—	—
GND_CP	P1	Power	I	Charge Pump Ground. Ground reference for amplifiers charge pump.	—	—
GND_HS	K2	Power	I	Headset Ground. Ground reference for the internal headset analog circuits.	—	—
GND_IO	P2	Power	I	IO Ground. Ground reference for IO circuits.	—	—
GPIO1/IRQ	B3	VIO	I/O	General Purpose Input/Output. Interrupt output. Programmable, open-drain, active-low programmable interrupt output.	Hi-Z	Hi-Z
GPIO2/ASP BCLK/SWDCLK	E4	VIO	I/O	General Purpose Input/Output. ASP Bit Clock. Serial shift clock for the interface. Serial Wire Debug Clock.	Weak pull down	Weak pull down
GPIO3/SPDIF TX/ASP_FSYNC/ SWDIO	N3	VIO	I/O	General Purpose Input/Output. S/PDIF Audio Serial Data Output. Serial data output for S/PDIF interface. ASP Frame Sync Clock. Identifies the start of each serialized PCM data word and indicates which channel, left or right, is active on the serial PCM audio data lines or indicates the start of each TDM frame. Serial Wire Debug I/O.	Weak pull down	Weak pull down
HS3	G4	VDD_P	I	Headset Connection. Input to headset and mic-button detection functions.	—	—
HS3_REF	F3	VDD_P	I	Headset Connection Reference. Input to pseudodifferential amplifier 1 and 2 output reference. This pin should be treated as a Kelvin connection to HS3 and routed out separately from HS3 to the headset jack if possible.	—	—
HS4	G1	VDD_P	I	Headset Connection. Input to headset and mic-button detection functions.	—	—

Table 1-1. WLCSP Pin Descriptions (Cont.)

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
HS4_REF	F2	VDD_P	I	Headset Connection Reference. Input to pseudodifferential amplifier 1 and 2 output reference. This pin should be treated as a Kelvin connection to HS4 and routed out separately from HS4 to the headset jack if possible.	—	—
HSBIAS_FILT	E1	VDD_P	I	Headset Bias Source Voltage Filter. Filter connection for the internal bias voltage used for headset bias.	—	—
HSBIAS_FILT_REF	D2	VDD_P	I	Headset Bias Source Voltage Filter Reference. Input of filter connection for the internal headset bias voltage.	—	—
I2C_SCL	E3	VIO	I	I2C Clock. Clock input for the I2C interface.	Hi-Z	Hi-Z
I2C_SDA	E2	VIO	I/O	I2C Input/Output. Data input/output for the I2C interface.	Hi-Z	Hi-Z
LDO_VD_FILT	M4	VDD_A	O	Digital Core Power Supply LDO output. Power supply for internal digital circuits. Must not be connected to any external loads.	—	—
PDM1_CLK OUT/SWDCLK	C4	VIO	I/O	PDM 1 Bit Clock Output. Serial Wire Debug Clock.	Weak pull down	Weak pull down
PDM1_DIN/ SWDIO	D3	VIO	I/O	PDM 1 Data Input. Serial Wire Debug I/O.	Weak pull down	Weak pull down
PDM2_CLK OUT/ASP_DOUT	J2	VIO	O	PDM 2 Bit Clock Output. ASP Data Output. Output for two's complement serial PCM audio data.	Weak pull down	Weak pull down
PDM2_DIN/ASP_DIN	H2	VIO	I	PDM 2 Data Input. ASP Data Input. Input for two's complement serial PCM audio data.	Weak pull down	Weak pull down
RESET	N2	VDD_P	I	Reset. The device enters a low power mode when this pin is driven low.	Weak pull down	—
RING_SENSE	P3	VDD_P	I	Ring Sense Input. Sense pin to detect headphone plug. Can be configured to be debounced on plug and unplug events independently.	—	—
SWIRE_CLK/ MCLK_IN	J4	VIO	I	SoundWire Serial Clock Input. Clock input to the SoundWire peripheral interface. Main Clock Input. Clock source for the device core, serial port mastering, and converters.	Weak pull down	Hi-Z
SWIRE_DATA0/ GPI4	H3	VIO	I/O	SoundWire Serial Data Input and Output 0. Primary serial data input and output of the SoundWire peripheral interface. General Purpose Input.	Weak pull down	Hi-Z
SWIRE_DATA1/ GPI5	J3	VIO	I/O	SoundWire Serial Data Input and Output 1. Serial data input and output of the SoundWire peripheral interface. General Purpose Input.	Weak pull down	Hi-Z
TIP_SENSE	J1	VDD_P	I	Tip Sense. Sense pin to detect headphone plug. Can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	—
VDD_A	L3	Power	I	Analog Supply. Power supply for amplifiers 1 and 2 charge pump and analog supply circuitry.	—	—
VDD_P	R4	Power	I	High Voltage Supply. Power supply for the high voltage interface.	—	—
VIO	K4	Power	I	I/O Power Supply. Power supply for external interface and internal digital logic.	—	—
VREF_FILT	C1	VDD_A	I	Voltage Reference. Reference voltage for internal ADCs and amplifiers' circuitry.	—	—

1.3 Termination of Unused Pins

Some systems may not need to connect to all of the device pins. [Table 1-2](#) shows the recommended termination for any permanently unused pins. A pin that is connected to other circuits but is only occasionally active is not required to follow the terminations shown.

Table 1-2. Recommended Termination of Unused Pins

Pin Name	Termination
IRQ/GPIO1	Float
GPIO3/SPDIF_TX	
AMP1_OUT	
AMP2_OUT	
ASP_BCLK	
ASP_FSYNC	
ASP_DOUT	
ASP_DIN	Grounded
HSBIAS_FILT	
PDM1_CLK_OUT	
PDM2_CLK_OUT	
PDM1_DIN	
PDM2_DIN	
ADC1_IN1_P	
ADC1_IN2_P	
ADC1_IN_N	
ADC2_IN_P	
ADC2_IN_N	
HS3	
HS3_REF	
HS4	
HS4_REF	
HSBIAS_FILT_REF	
ADDR	
TIP_SENSE	
RING_SENSE	
SWIRE_CLK/MCLK_IN	
SWIRE_DATAx	
I2C_SCL	Grounded or Tie to HS_BIAS_FILT_REF
I2C_SDA	
RESET	Pulled high
GPIO2	Float or Tie to VIO

1.4 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS42L45 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to JEDEC ESD protection standards JS-001-2017 and JS-001-2018.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	Left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Signal-to-noise-floor ratio (SNR)	The ratio of the rms value of all the spectral components of the muted output over the specified measurement bandwidth relative to a full-scale output signal.
Gain drift	The change in gain value with temperature, expressed in ppm/°C units.
Gain accuracy	The difference between the actual gain and the nominal gain.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel gain mismatch	The gain difference between left and right channel pairs. Interchannel gain mismatch is expressed in dB.
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Offset error	The deviation of the midscale transition (111...111 to 000...000) from the ideal.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion (THD)	The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth ¹ relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz or 20 Hz–80 kHz) relative to the rms value of the signal. THD+N is measured at –1 dBFS for the analog input and at 0 dB (or as otherwise specified in the table) for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.

1. All performance measurements are specified with a 20 kHz low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise):

- Ground = GND_A = GND_IO = GND_CP = GND_HS = 0 V, voltages are with respect to ground.

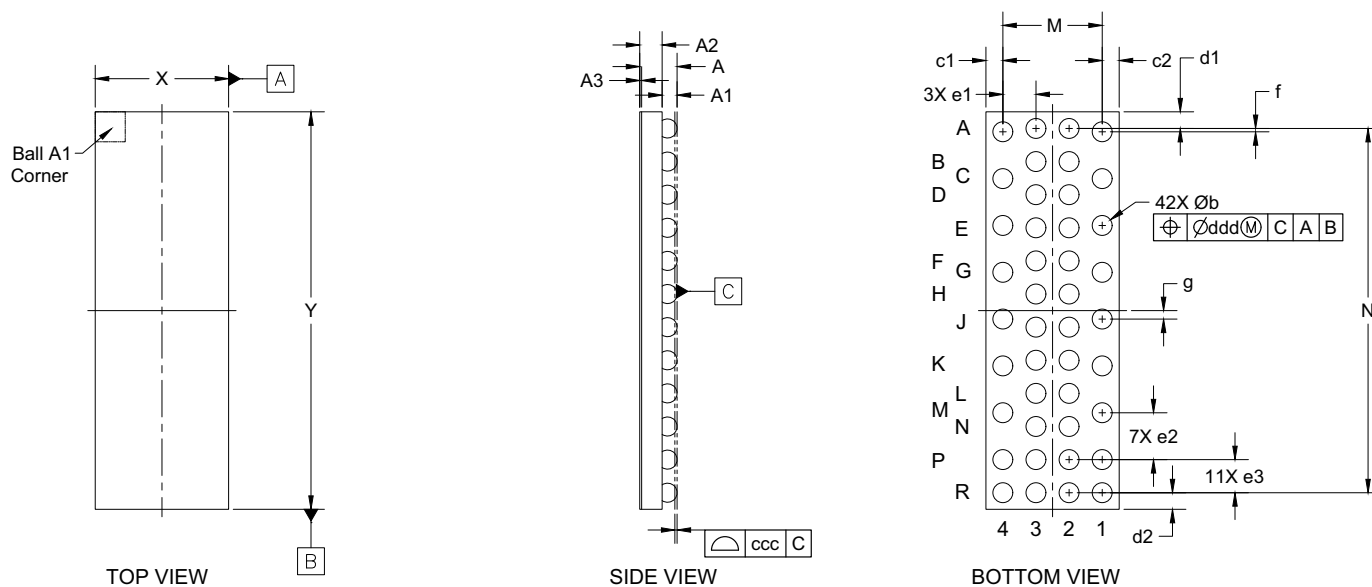
Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump and analog	VDD_A	1.66	1.94	V
	Serial interface control port	1.8 V nominal VIO	1.66	1.94	V
		1.2 V nominal VIO	1.10	1.30	V
	Main power supply	Functional range 1,2 VDD_P	3.20	3.6	V
			3.30	3.6	V
			Parametric performance range 3		3.6
Parametric performance with stereo HS MIC support 4			3.6	V	
External voltage applied to pin 5,6		TIP_SENSE pin V _{TIPSENSE}	CP_FILT_N	VDD_P	V
CP_FILT_P/N domain pins		V _{CP_FILT}	CP_FILT_N	VDD_P	V
VIO domain pins		V _{VIO}	0	VIO	V
VDD_A domain pins		V _{VDD_A}	0	VDD_A	V
VDD_P domain pins		V _{VDD_P}	0	VDD_P	V
RING_SENSE pin		V _{RINGSENSE}	0	VDD_P	V
Ambient temperature		T _A	−40	+85	°C

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and/or parametric performance are not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. Defined as the range that the CS42L45 is capable of operating functionally, but may not meet all parametric specifications.
2. The following are affected when VDD_P < 3.0 V: HSBias, charge pump LDO, TIP_SENSE threshold, and RING_SENSE threshold.
3. Defined as the range that the CS42L45 is capable of operating functionally, and meets all parametric specifications.
4. To support unplug detection of a stereo MIC jack if MICBIAS is set to 2.75 V, VDD_P must be at least 3.3 V.
5. The maximum over/undervoltage is limited by the input current.
6. [Section 1.2](#) lists the power supply domain in which each CS42L45 pin resides.

4 Package Dimensions

4.1 WLCSP Package Dimensions



Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.4700	0.50000	0.5300
A1	0.1850	0.20000	0.2150
A2	0.2850	0.30000	0.3150
A3	REF	0.02500	REF
b	0.2350	0.26500	0.2950
c1	REF	0.22730	REF
c2	REF	0.22730	REF
d1	REF	0.22255	REF
d2	REF	0.22245	REF
e1	BSC	0.44300	BSC
e2	BSC	0.62650	BSC
e3	BSC	0.44300	BSC
f	REF	0.04450	REF
g	REF	0.11405	REF
M	BSC	1.32900	BSC
N	BSC	4.87300	BSC
X	1.7586	1.78360	1.8086
Y	5.2930	5.31800	5.3430
ccc=0.03			
ddd=0.015			

Notes: Controlling dimension is millimeters.

Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum X/Y Tolerances can apply to an individual edge increasing or decreasing by 25µm.

Figure 4-1. WLCSP Package Dimensions

5 Ordering Information

Table 5-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS42L45	PC Codec with 2 V _{RMS} -capable Headphone Driver	42-ball WLCSP	Yes	Commercial	–40 °C to +85 °C	Tape and Reel	CS42L45-DWR

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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