

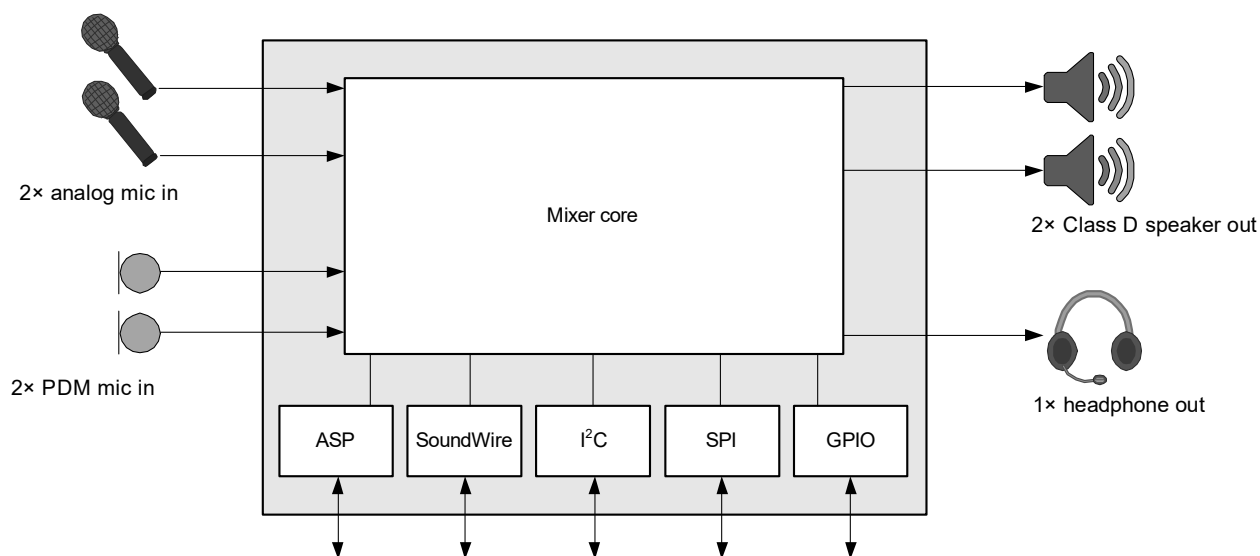
PC Codec with Headphone, MIC Interface, and Class D Speaker Drivers

System Features

- Stereo headphone (HP) output with 114 dB dynamic range
 - Class H headphone amplifier with automatic or manual supply adjust
 - 2×33.7 mW power output at -85 dB THD+N into 30Ω
 - $1 V_{RMS}$ output swing into 30Ω loads
 - Load detection
- Mono mic/stereo line input with 94 dB dynamic range
 - Headset bias with integrated bias resistor
 - $1 V_{RMS}$ input voltage
 - Programmable analog front end (AFE) gain from -6 dB to $+18$ dB in 6 dB steps
- Integrated detect features
 - OMTP (Open Mobile Terminal Platform) and CTIA headset-type detection and configuration with low-impedance internal switches
 - Mic button press detect with ADC automute
 - Mic button detection compatible with Android Wired Headset Specification (Version 1.1)
 - Automatic Hi-Z of headset bias output on headset bias current drop or HP/headset unplug
- Stereo Class D Bridge-tied load (BTL) speaker driver
 - $2 W @ 1 \%$ THD+N into 4Ω load
 - 102 dB dynamic range
- System wake from headset/headphone plug/unplug or mic button press
- Enhanced audio processing including EQ, LHPF, and DRC
- I²C control supporting rates up to 1 Mbit/s
- MIPI® SoundWire® v1.3 interface with SDCA v1.1 support
- S/PDIF transmit (Sony/Philips digital interface format)
- Integrated fractional PLL
 - Allows multiple clock input rates
 - Reference clock sourced from either SoundWire clock or external MCLK_IN source
- PDM input for digital microphones with support for decimation rates up to 96 kHz
- Audio serial port (ASP)
 - I²S (two channels) or TDM (up to six channels)
 - Controller or Target Mode
 - Sample rate support for 8 kHz to 192 kHz
- SPI master for connection and control of auxiliary devices
- Integrated power management
 - Digital core can be supplied externally, or by an internal LDO from the VDD_IO supply
 - Step-up/down charge pump improves HP efficiency
 - VDD_P monitor to detect and report brownout conditions

Applications

- Laptops
- Desktops
- Ultrabooks
- Chromebooks



General Description

The CS42L43B is an audio codec with integrated MIPI SoundWire interface (Version 1.3 compliant), I²C, SPI, and I²S/TDM interfaces designed for portable applications. It provides a high dynamic range, stereo DAC for headphone output, two integrated Class D amplifiers for loudspeakers, and two ADCs for wired headset microphone input or stereo line input. PDM inputs are provided for digital microphones. Each PDM input has two channels, and each channel has three paths with individual volume controls. All four digital microphone paths and both ADC paths are available simultaneously.

The CS42L43B provides high performance audio capture from the ADC and PDM inputs and audio playback to the headphone DACs, Class D speaker drivers, and an IEC-60958-3-compatible S/PDIF transmitter. The CS42L43B includes assignable sample-rate converters (SRCs) and the following enhanced audio processing capabilities:

- An assignable stereo three-band parametric equalizer
- Four channels of five-band parametric equalizer
- Four channels of low- and high-pass filtering
- Four channels of dynamic range control

Digital mixers are available with independent attenuation on each mixer input.

Digital volume/mute control is available on all capture and playback paths and selectable high-pass filters are available on the capture paths for removal of DC offsets or wind noise suppression.

A headset mic bias with an integrated pull-up resistor is provided for use with the headset interface. Other headset features include automatic headset type detection (OMTP/CTIA-compliant), mic-bias/ground switching, and headset-button detection including *3.5 mm headset jack: Device specification*. Other features include insert/removal detection, headphone load impedance detection, and stereo line-in support.

The CS42L43B can be configured to provide a bridge from a SoundWire host to the SPI master and ASP ports. This enables non-SoundWire audio peripherals such as additional speaker amplifiers or a companion DSP to be integrated alongside a SoundWire host system.

A high-performance fractional PLL is available for generating internal audio sample clocks.

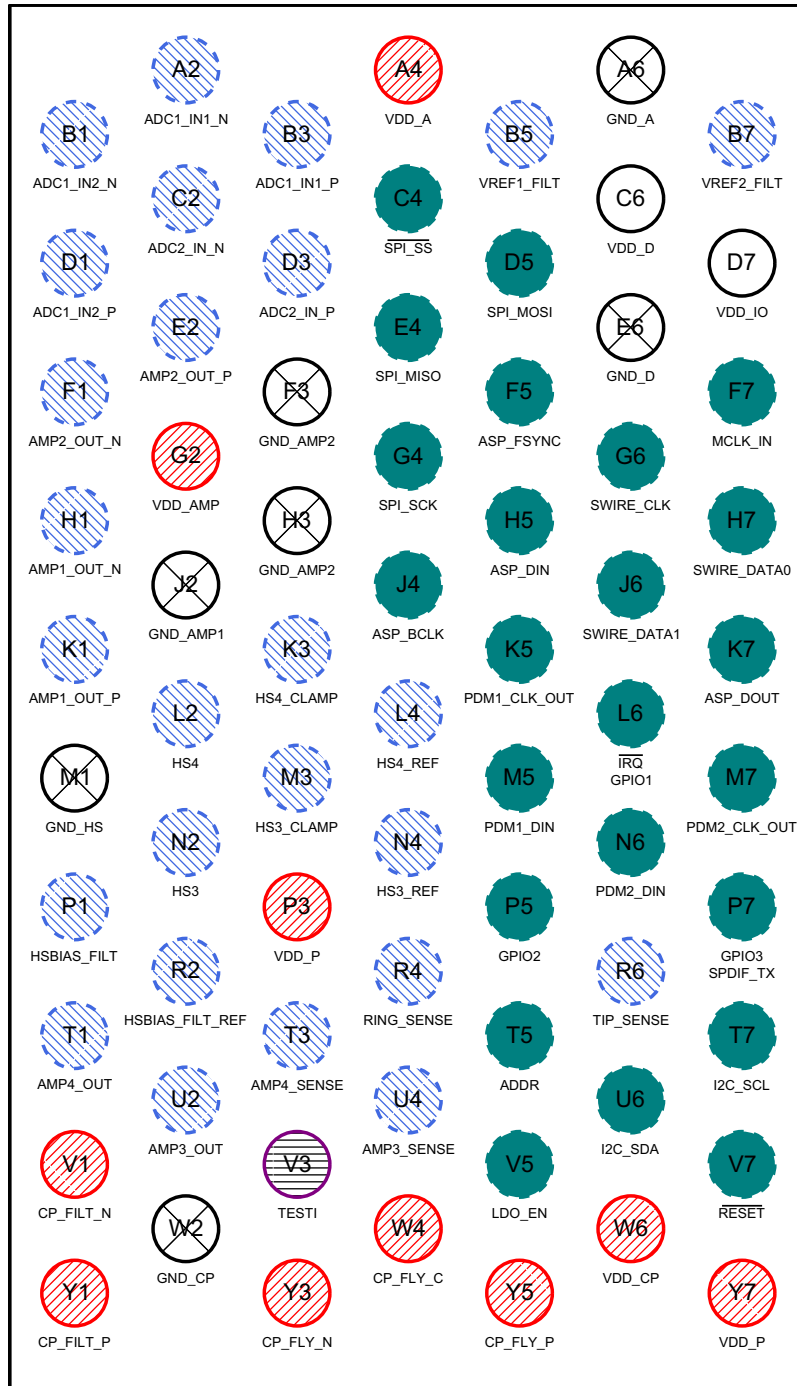
The CS42L43B is available in a commercial-grade, 70-ball WLCSP (wafer-level chip scale package) for operation between –40 °C to +85 °C. The WLCSP package can be routed using standard PCB with vias in many applications.

See [Section 5](#) for ordering information.

1 Pin Assignments and Descriptions

This section shows pin assignments and describes pin functions.

1.1 WLCSP Pin Out (Through-Package, Top View)



Not to scale



Figure 1-1. WLCSP Pin Diagram (Through-Package, Top View)

1.2 WLCSP Pin Descriptions

Table 1-1. WLCSP Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
ADC1_IN1_N	A2	VDD_P	I	Inverting analog input for ADC 1 mux input 1.	—	—
ADC1_IN1_P	B3	VDD_P	I	Non-inverting analog input for ADC 1 mux input 1.	—	—
ADC1_IN2_N	B1	VDD_P	I	Inverting analog input for ADC 1 mux input 2.	—	—
ADC1_IN2_P	D1	VDD_P	I	Non-inverting analog input for ADC 1 mux input 2.	—	—
ADC2_IN_N	C2	VDD_P	I	Inverting analog input for ADC 2.	—	—
ADC2_IN_P	D3	VDD_P	I	Non-inverting analog input for ADC 2.	—	—
ADDR	T5	VDD_IO	I	Address select for I²C and SoundWire. Address pin for the I ² C target address and the SoundWire Unique ID. Latched on POR, hard, or soft reset. Connect this pin to VDD_IO or GND.	Weak pull down	Weak pull down
AMP1_OUT_N	H1	VDD_AMP	O	Amplifier 1 (Left) Negative Output. This amplifier drives the negative side of a differentially connected low-impedance speaker.	—	—
AMP1_OUT_P	K1	VDD_AMP	O	Amplifier 1 (Left) Positive Output. This amplifier drives the positive side of a differentially connected low-impedance speaker.	—	—
AMP2_OUT_N	F1	VDD_AMP	O	Amplifier 2 (Right) Negative Output. This amplifier drives the negative side of a differentially connected low-impedance speaker.	—	—
AMP2_OUT_P	E2	VDD_AMP	O	Amplifier 2 (Right) Positive Output. This amplifier drives the positive side of a differentially connected low-impedance speaker.	—	—
AMP3_OUT	U2	CP_FILT_P/ N	O	Amplifier 3 Output. Ground-centered audio output typically used for headphone speakers and connects to TIP (HS1).	—	—
AMP3_SENSE	U4	CP_FILT_P/ N	I	Amplifier 3 Feedback Sense Input.	—	—
AMP4_OUT	T1	CP_FILT_P/ N	O	Amplifier 4 Output. Ground-centered audio output typically used for headphones and connects to RING1 (HS2).	—	—
AMP4_SENSE	T3	CP_FILT_P/ N	I	Amplifier 4 Feedback Sense Input.	—	—
ASP_BCLK	J4	VDD_IO	I/O	ASP Bit Clock. Serial shift clock for the interface.	Weak pull down	Weak pull down
ASP_DIN	H5	VDD_IO	I	ASP Data Input. Input for two's complement serial PCM audio data.	Weak pull down	Weak pull down
ASP_DOUT	K7	VDD_IO	O	ASP Data Output. Output for two's complement serial PCM audio data.	Weak pull down	Weak pull down
ASP_FSYNC	F5	VDD_IO	I/O	ASP Frame Sync Clock. In I ² S Mode, identifies the start of each serialized PCM data word and indicates which channel, left or right, is active on the serial PCM audio data lines. In TDM Mode, indicates the start of each TDM frame.	Weak pull down	Weak pull down
CP_FILT_N	V1	Power	O	Inverting Charge Pump Filter Connection. Power supply for the inverting charge pump that provides the negative rail for amplifiers 3 and 4.	—	—
CP_FILT_P	Y1	Power	O	Step-Up/Down Charge Pump Filter Connection. Power supply for the step-up/down charge pump that provides the positive rail for amplifiers 3 and 4.	—	—
CP_FLY_C	W4	VDD_P	O	Charge Pump Cap Common Node. Common positive node for the step-down and inverting charge pumps' flying capacitors of amplifiers 3 and 4.	—	—
CP_FLY_N	Y3	CP_FILT_P	O	Charge Pump Cap Negative Node. Negative node for the step-up/down charge-pump flying capacitor of amplifiers 3 and 4.	—	—
CP_FLY_P	Y5	VDD_P	O	Charge Pump Cap Positive Node. Positive node for the step-up/down charge-pump flying capacitor of amplifiers 3 and 4.	—	—

Table 1-1. WLCSP Pin Descriptions (Cont.)

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
GND_A	A6	Power	I	Analog Ground. Ground reference for the internal analog circuits.	—	—
GND_AMP1	J2	Power	I	Amplifier 1 (Left) Output Ground. This amplifier drives a low-impedance speaker.	—	—
GND_AMP2	F3, H3	Power	I	Amplifier 2 (Right) Output Ground. This amplifier drives a low-impedance speaker.	—	—
GND_CP	W2	Power	I	Charge Pump Ground. Ground reference for the charge pump of amplifiers 3 and 4.	—	—
GND_D	E6	Power	I	Digital Ground. Ground reference for the internal digital circuits.	—	—
GND_HS	M1	Power	I	Headset Ground. Ground reference for the internal headset analog circuits.	—	—
GPIO2	P5	VDD_IO	I/O	General Purpose Input/Output 2.	Weak pull down	Weak pull down
GPIO3/SPDIF_TX	P7	VDD_IO	I/O	General Purpose Input/Output 3. S/SPDIF Audio Serial Data Output. Serial data output for S/SPDIF interface.	Weak pull down	Weak pull down
HS3	N2	VDD_P	I	Headset Connection. Input to headset and mic-button detection functions.	—	—
HS3_CLAMP	M3	VDD_P	I	Headset Depletion FET Connections. Input to drain of integrated depletion FET for ground-noise rejection.	—	—
HS3_REF	N4	VDD_P	I	Headset Connection Reference. Input to pseudodifferential amplifier 3 and 4 output reference.	—	—
HS4	L2	VDD_P	I	Headset Connection. Input to headset and mic-button detection functions.	—	—
HS4_CLAMP	K3	VDD_P	I	Headset Depletion FET Connections. Input to drain of integrated depletion FET for ground-noise rejection.	—	—
HS4_REF	L4	VDD_P	I	Headset Connection Reference. Input to pseudodifferential amplifier 3 and 4 output reference.	—	—
HSBIAS_FILT	P1	VDD_P	I	Headset Bias Source Voltage Filter. Filter connection for the internal bias voltage used for headset bias.	—	—
HSBIAS_FILT_REF	R2	VDD_P	I	Headset Bias Source Voltage Filter Reference. Input of filter connection for the internal headset bias voltage.	—	—
I2C_SCL	T7	VDD_IO	I	I2C Clock. Clock input for the I2C interface.	Weak pull down	Weak pull down
I2C_SDA	U6	VDD_IO	I/O	I2C Input/Output. Data input/output for the I2C interface.	Weak pull up	Weak pull up
IRQ/GPIO1	L6	VDD_IO	I/O	Interrupt output. Programmable, open-drain, active-low programmable interrupt output. General Purpose Input/Output 1.	Weak pull up	Weak pull up
LDO_EN	V5	VDD_P	I	LDO Enable. Digital core logic LDO enable.	Weak pull down	Weak pull down
MCLK_IN	F7	VDD_IO	I	Main Clock Input. Clock source for the device core, serial port mastering, and converters.	Weak pull down	Weak pull down
PDM1_CLK_OUT	K5	VDD_IO	O	PDM 1 Bit Clock Output.	Weak pull down	Weak pull down
PDM1_DIN	M5	VDD_IO	I	PDM 1 Data Input.	Weak pull down	Weak pull down
PDM2_CLK_OUT	M7	VDD_IO	O	PDM 2 Bit Clock Output.	Weak pull down	Weak pull down
PDM2_DIN	N6	VDD_IO	I	PDM 2 Data Input.	Weak pull down	Weak pull down
RESET	V7	VDD_P	I	Reset. The device enters a low power mode when this pin is driven low.	Weak pull down	Weak pull down

Table 1-1. WLCSP Pin Descriptions (Cont.)

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
RING_SENSE	R4	VDD_P	I	Ring Sense Input. Sense pin to detect headphone plug. Can be configured to be debounced on plug and unplug events independently.	—	—
SPI_MISO	E4	VDD_IO	I	SPI Slave Out Master In. SPI serial data where the slave device is the transmitter and the master device is the receiver.	Weak pull down	Weak pull down
SPI_MOSI	D5	VDD_IO	O	SPI Master Out Slave In. SPI serial data where the master device is the transmitter and the slave device is the receiver.	Weak pull down	Weak pull down
SPI_SCK	G4	VDD_IO	O	SPI Serial Data Clock. The bit clock for the data on the SPI_MOSI and SPI_MISO pins.	Weak pull down	Weak pull down
SPI_SS	C4	VDD_IO	O	SPI Slave Select. SPI slave device select.	Weak pull up	Weak pull up
SWIRE_CLK	G6	VDD_IO	I	SoundWire Serial Clock Input. Clock input to the SoundWire peripheral interface.	Weak pull down	Weak pull down
SWIRE_DATA0	H7	VDD_IO	I/O	SoundWire Serial Data Input and Output 0. Primary serial data input and output of the SoundWire peripheral interface.	Weak pull down	Weak pull down
SWIRE_DATA1	J6	VDD_IO	I/O	SoundWire Serial Data Input and Output 1. Serial data input and output of the SoundWire peripheral interface.	Weak pull down	Weak pull down
TESTI	V3	—	I	Test Input Pin. Must be connected to ground.	—	—
TIP_SENSE	R6	VDD_P	I	Tip Sense. Sense pin to detect headphone plug. Can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	—
VDD_A	A4	Power	I	Analog Power Supply. Power supply for internal analog circuits.	—	—
VDD_AMP	G2	Power	I	Amplifiers 1 and 2 Power Supply.	—	—
VDD_CP	W6	Power	I	Charge Pump Power. Power supply for the charge pump of amplifiers 3 and 4.	—	—
VDD_D	C6	Power	I	Digital Core Power Supply. Power supply for internal digital circuits.	—	—
VDD_IO	D7	Power	I	I/O Power Supply. Power supply for external interface and internal digital logic.	—	—
VDD_P	P3, Y7	Power	I	High-Voltage Supply. Power supply for the high voltage interface.	—	—
VREF1_FILT	B5	VDD_A	I	Voltage Reference. Reference voltage for internal ADCs and circuitry of amplifiers 3 and 4.	—	—
VREF2_FILT	B7	VDD_A	I	Voltage Reference. Reference voltage for internal circuitry of amplifiers 1 and 2.	—	—

1.3 Termination of Unused Pins

Some systems may not need to connect to all of the device pins. [Table 1-2](#) shows the recommended termination for any permanently unused pins. A pin that is connected to other circuits but is only occasionally active is not required to follow the terminations shown.

Table 1-2. Recommended Termination of Unused Pins

Pin Name	Termination
IRQ/GPIO1 GPIO3/SPDIF_TX	Float
AMP1_OUT_P/N AMP2_OUT_P/N AMP3_OUT AMP4_OUT	
ASP_BCLK ASP_FSYNC ASP_DOUT ASP_DIN	
HSBIAS_FILT	
PDM1_CLK_OUT PDM2_CLK_OUT PDM1_DIN PDM2_DIN	
SPI_MOSI SPI_SCK SPI_SS	
ADC1_IN1_P/N ADC1_IN2_P/N ADC2_IN_P/N	Grounded
AMP3_SENSE ¹ AMP4_SENSE ²	
HS3 HS3_CLAMP HS3_REF HS4 HS4_CLAMP HS4_REF HSBIAS_FILT_REF	
ADDR I2C_SCL I2C_SDA	
MCLK_IN	
TIP_SENSE RING_SENSE	
TEST1	
SPI_MISO	
SWIRE_CLK SWIRE_DATAx	
NC	
VDD_AMP ³	
RESET	Can be tied to VDD_IO or VDD_P
GPIO2	Float or Tie to VDD_IO

1. AMP3_SENSE must be grounded if AMP3_OUT is unused.

2. AMP4_SENSE must be grounded if AMP4_OUT is unused.

3. VDD_AMP must be grounded if AMP1 and AMP2 are unused.

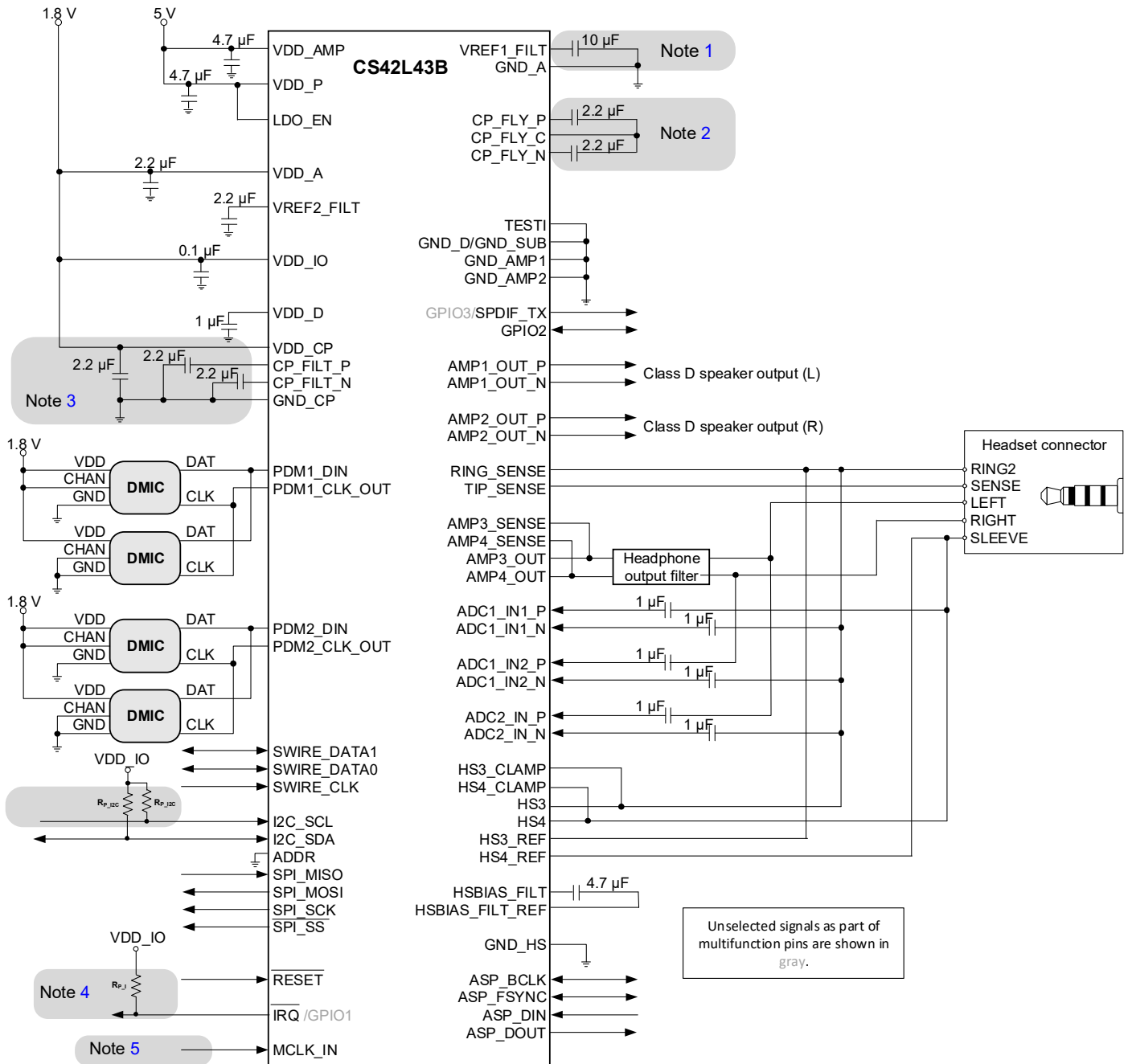
1.4 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS42L43B is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to JEDEC ESD protection standards JS-001-2017 and JS-001-2018.

2 Typical Connections

2.1 Typical Connection Diagrams



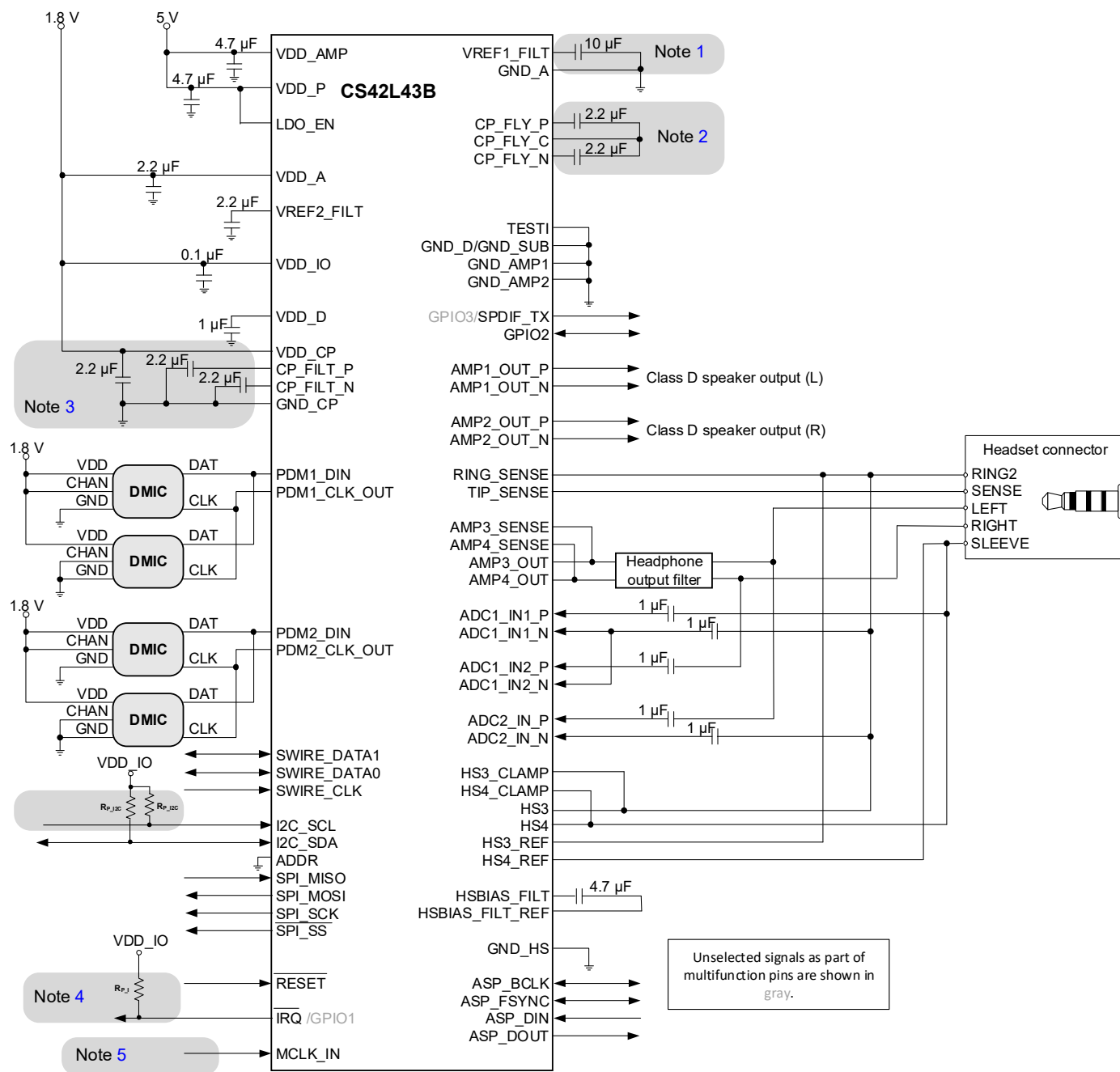


Figure 2-2. Typical Connection Diagram—Non-DSP Use Case, Shared ADC1 Ground

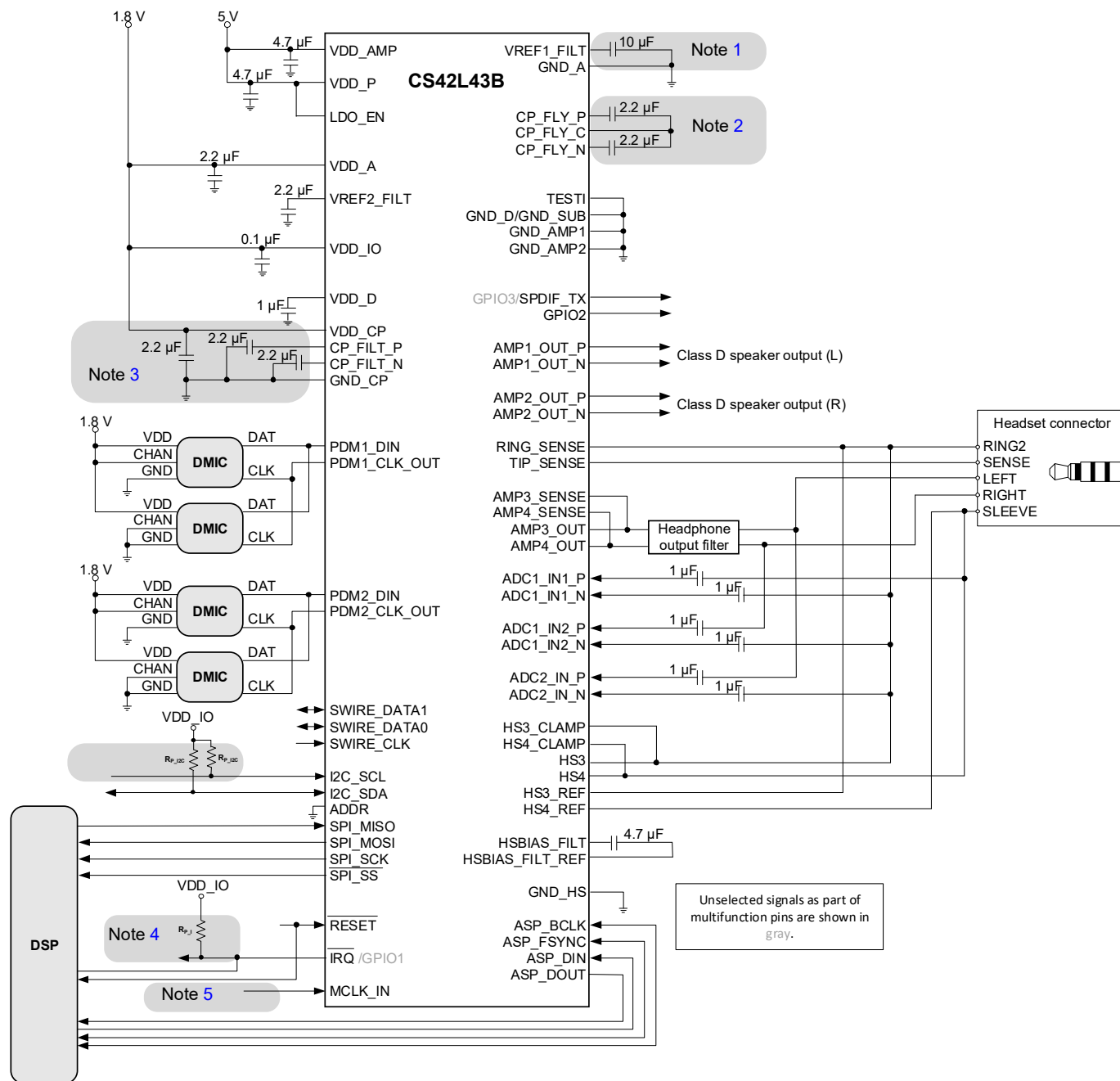


Figure 2-3. Typical Connection Diagram—DSP Use Case

Notes:

1. Lowering capacitance below the value shown affects PSRR, THD+N, ADC-DAC isolation and intermodulation, and interchannel isolation and intermodulation.
2. Avoid series resistance in the path of the power supplies. Any voltage drop on the charge pump fly nodes directly affects the charge-pump supplies and clips the audio output.
3. The headphone amplifier's output power and distortion ratings use the nominal capacitances shown. Larger capacitance reduces ripple on the internal amplifiers' supplies and, in turn, reduces distortion at high-output power levels. Smaller capacitance may not reduce ripple enough to achieve output power and distortion ratings. Because actual values of typical X7R/X5R ceramic capacitors deviate from nominal values by a percentage specified in the manufacturer's data sheet, capacitors must be selected for maximum output power and minimum distortion required. You can use higher-value capacitors than those shown; however, you must not use lower-value capacitors (values can vary from the nominal by $\pm 20\%$). A 0402-size or larger package is recommended.
4. A pull-up resistance of 10 k Ω or greater is recommended.
5. Connect to ground or a reference clock source.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	Left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range	The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Signal-to-noise-floor ratio (SNR)	The ratio of the RMS value of all the spectral components of the muted output over the specified measurement bandwidth relative to a full-scale output signal.
Gain drift	The change in gain value with temperature, expressed in ppm/°C.
Gain accuracy	The difference between the actual gain and the nominal gain.
Idle channel noise	The RMS value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel gain mismatch	The gain difference between left and right channel pairs, expressed in dB.
Interchannel isolation	A measure of crosstalk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Offset error	The deviation of the midscale transition (111...111 to 000...000) from the ideal.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion (THD)	The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth ¹ relative to the RMS amplitude of the fundamental (that is, test frequency) output.
Total harmonic distortion + noise (THD+N)	The ratio of the RMS sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz to 20 kHz or 20 Hz to 80 kHz) relative to the RMS value of the signal. THD+N is measured at –1 dBFS for the analog input and at 0 dB (or as otherwise specified in the table) for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.

1. All performance measurements are specified with a 20 kHz low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

Table 3-2. Recommended Operating Conditions

Test conditions: Ground = GND_A = GND_D = GND_CP = GND_AMP1/2 = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump	VDD_CP	1.66	1.94	V
	LDO regulator for digital ¹	LDO_EN = 0 VDD_D	1.10	1.30	V
	Serial interface control port	1.8 V nominal VDD_IO	1.66	1.94	V
	Analog	VDD_A	1.66	1.94	V
	Main power supply	Functional range ^{2,3} Parametric performance range ⁴ Parametric performance with stereo HS MIC support ⁵ VDD_P	2.50	5.25	V
			3.20	5.25	V
			3.30	5.25	V
	Class D supplies	VDD_AMP	4.75	5.25	V
External voltage applied to pin ^{6,7}	TIP_SENSE pin	V_TIPSENSE	CP_FILT_N	VDD_P	V
	CP_FILT_P/N domain pins	V_CP_FILT	CP_FILT_N	VDD_P	V
	VDD_IO domain pins	V_VDD_IO	0	VDD_IO	V
	VDD_A domain pins	V_VDD_A	0	VDD_A	V
	VDD_P domain pins	V_VDD_P	0	VDD_P	V
	RING_SENSE pin	V_RINGSENSE	0	VDD_P	V

Table 3-2. Recommended Operating Conditions (Cont.)

Test conditions: Ground = GND_A = GND_D = GND_CP = GND_AMP1/2 = 0 V; voltages are with respect to ground.

Parameter	Symbol	Minimum	Maximum	Unit
Ambient temperature	T _A	–40	+85	°C
Functional range ² Parametric performance range ⁴		–10	+70	°C
VDD_AMP supply ramp rate	—	0.0017	0.1	V/μs

Note: Functionality and/or parametric performance are not guaranteed or implied outside of the limits in this table. Operation outside of these limits may adversely affect device reliability.

1. If LDO_EN is asserted, no external voltage must be applied to VDD_D and VDD_IO must be within the recommended operating range specified in Table 3-2. When LDO_EN is asserted, the VDD_D pin outputs 1.2 V. The minimum high input for LDO_EN is 1.2 V. It can be connected to 1.2 V, 1.8 V, 3.3 V, or 5 V supplies to enable the LDO.
2. Defined as the range that the CS42L43B is capable of operating functionally, but may not meet all parametric specifications.
3. The following are affected when VDD_P < 3.0 V: HSBias, charge pump LDO, TIP_SENSE threshold, and RING_SENSE threshold.
4. Defined as the range that the CS42L43B is capable of operating functionally, and meets all parametric specifications.
5. To support unplug detection of a stereo MIC jack if MICBIAS is set to 2.75 V, VDD_P must be at least 3.3 V.
6. The maximum over/undervoltage is limited by the input current.
7. the power supply domain in which each CS42L43B pin resides.

4 Package Dimensions

4.1 WLCSP Package Dimensions

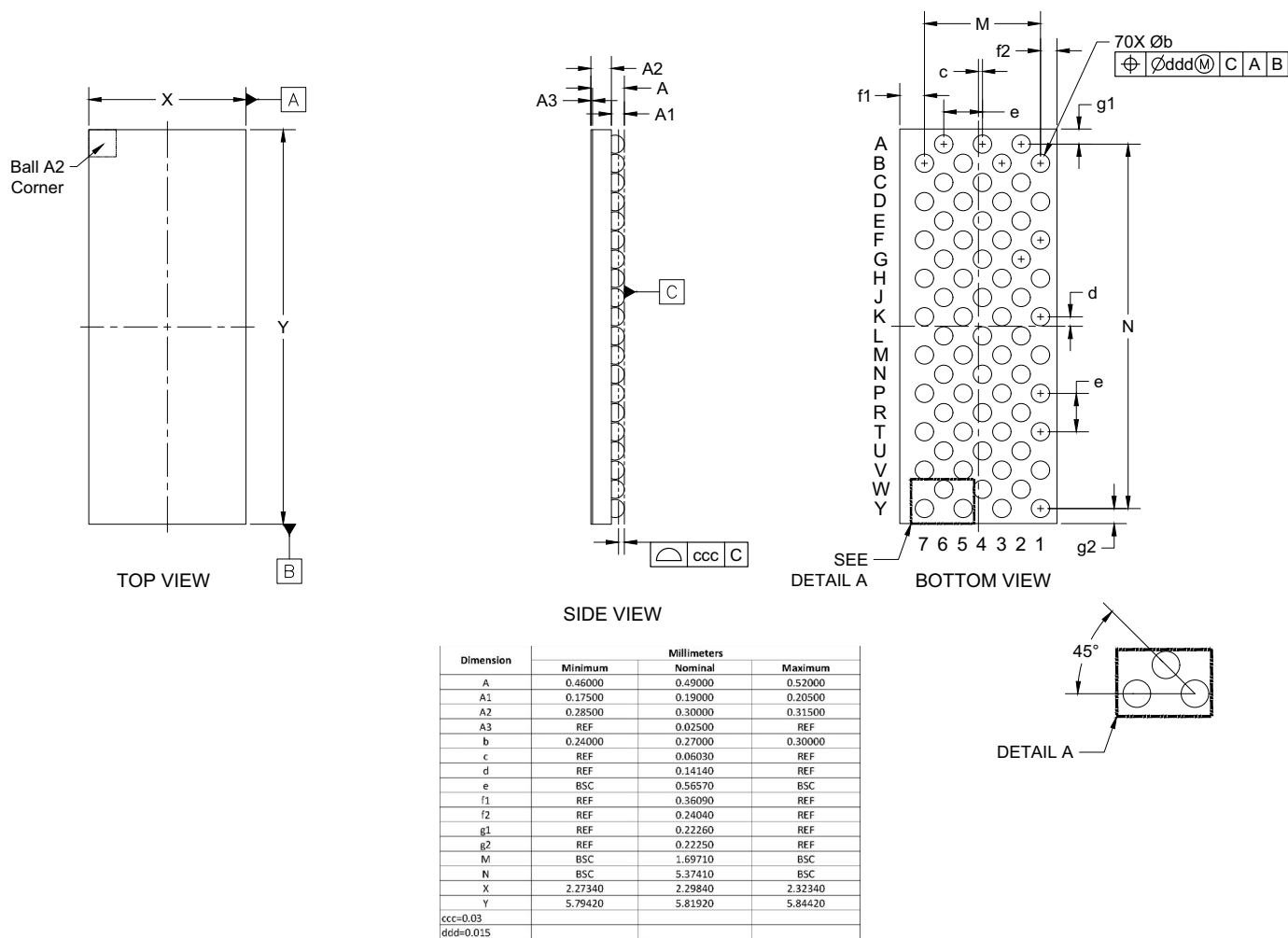


Figure 4-1. WLCSP Package Dimensions

5 Ordering Information

Table 5-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS42L43B	PC Codec with Headphone, MIC Interface, and Class D Speaker Drivers	70-ball WLCSP	Yes	Commercial	–40 °C to +85 °C	Tape and Reel	CS42L43B-DWR

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

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