

Advanced Haptic Driver with Waveform Memory, Integrated DSP, and Closed-Loop Algorithms

Features

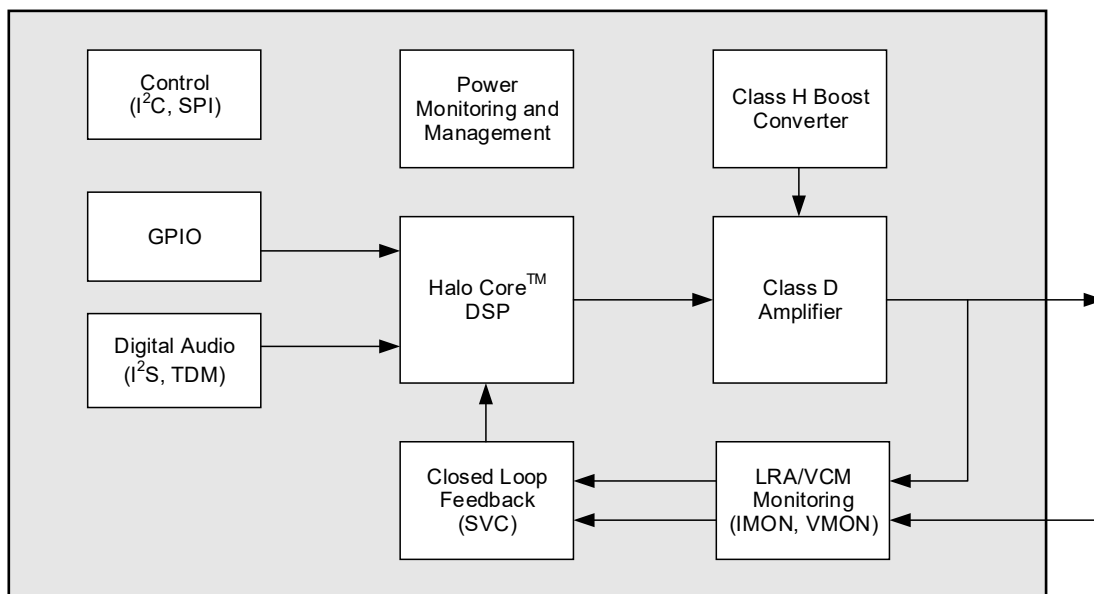
- Easy adoption and integration with LRA/VCM systems: pre-stored haptic waveforms and resonance-frequency calibration
- Flexible boost design with wide input-voltage range: supports universal design for 2S/3S/4S battery
- High-power output driver enables fast startup and braking
- 130 MIPS Halo Core™ digital signal processor (DSP)
- Runtime haptics enables dynamic haptic-waveform generation with minimized delays
- Dynamic F_0 and Re_{DC} tracking
- ROM/RAM-stored haptic waveforms triggered by I²C/SPI/GPIO for gaming and user-interface events
- Supply rail reactive brownout system protection
- Low-power modes with memory retention
- Internal clock generation: no external clock required
- Supports single-supply operation

Specifications

- 13.8 V_{PK} output (internal boost, 8 Ω load)
- 15.6 V_{PK} output (external supply, 8 Ω load)
- 5.0 V–18.5 V Class D amplifier supply
- 15 V internal boost output voltage
- 3.0 V–18.5 V internal boost supply
- Ultra-low power
 - 3.6 μ A current consumption in Reset State
 - 12 μ A current consumption in Hibernate State
- Ultra-low latency
 - 4.6 ms wake-to-haptics from Reset State
 - 3.3 ms wake-to-haptics from Hibernate State
- Support for 1.8 V and 3.3 V digital input/output
- 34-pin QFN package, 0.4 mm pin pitch
- 4 × 4.5 mm package size

Applications

- Trackpads
- Tablet/laptop PCs



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Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

General Description

The CS40L50 integrates a self-contained haptic signal generator and driver, optimized for high-performance haptic touchpad, virtual button, and gaming applications. The hardware and the digital signal processing are resonance-aware and designed specifically for optimal drive of highly resonant linear resonant actuators (LRAs) and voice coil motors (VCMs).

The CS40L50 incorporates a 130 MIPS Halo Core™ DSP, which is used to execute the haptic-control algorithms. Waveforms are stored in ROM or RAM to match the LRA/VCM characteristics. Ultra-low power reset and hibernate states enable always-on operation with fast wake-up via GPIO. ROM-defined waveforms can be output within 4.6 ms of wake up from reset. Additional waveforms can be downloaded to RAM during run time; these are retained in the low-power Hibernate State and can be output within 3.3 ms of wake-up from hibernate. Runtime haptic-waveform synthesis allows application-specific waveforms to be generated using PCM or PWLE-coded parameters.

The Class D amplifier supports supply voltages up to 18.5 V. The amplifier incorporates an advanced closed-loop architecture and a differential output stage. The digitally controlled boost converter supports Class-H tracking and generates up to 15 V output from typical system supply rails (e.g., 5 V or 12 V), or directly from 2S/3S/4S batteries. Using the internal-boost configuration, the CS40L50 delivers up to 13.8 V_{PK} into a 8 Ω load. Using an external supply, output up to 15.6 V_{PK} is possible.

The CS40L50 includes self-protection and system-protection features. The boost and driver stages are protected against short circuits; IC over-temperature shutdown protection is provided in hardware. Battery voltage is continuously monitored. The boost converter and driver gain are automatically adjusted to preserve battery voltage according to programmable voltage/current load-shedding set-points. The battery-protection adjustment of the driver is integrated with the IC thermal protection, ensuring seamless coordination of gain rollback if necessary.

The CS40L50 is available in a commercial-grade 0.4 mm pitch, 34-pin QFN package for operation from –40° to +85°C.

See [Section 6](#) for ordering information.

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1 Pin Assignments and Descriptions

1.1 34-Pin QFN (Top View, Through-Package)

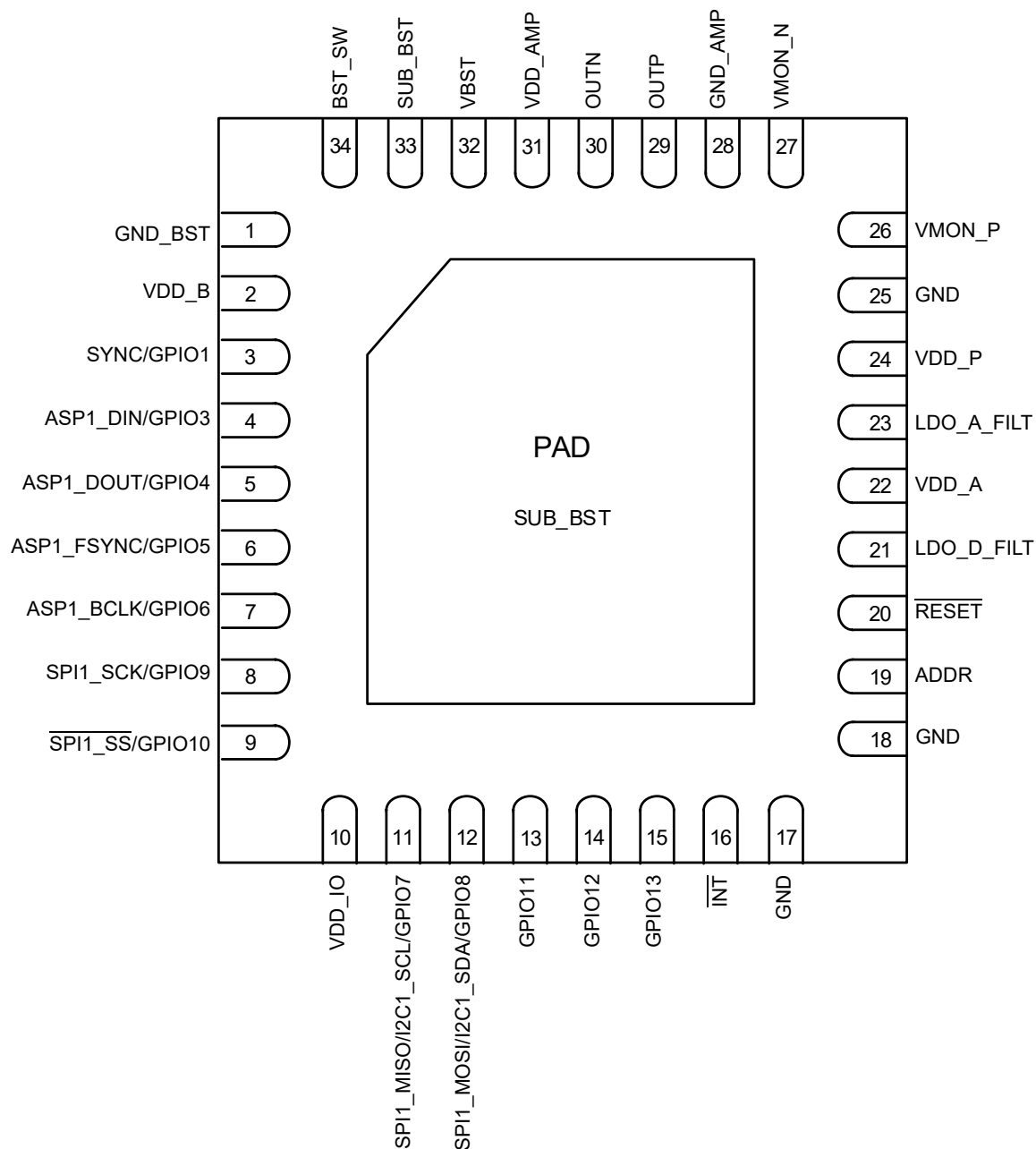


Figure 1-1. QFN 34-pin diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
Digital I/O						
ASP1_BCLK/GPIO6	7	VDD_IO	I/O	Audio Serial Port Bit Clock. Serial shift clock for ASP interface. Optional clock reference for PLL. GPIO6. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
ASP1_DIN/GPIO3	4	VDD_IO	I/O	Audio Serial Port Data Input. Serial data input for ASP interface. GPIO3. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
ASP1_DOUT/GPIO4	5	VDD_IO	I/O	Audio Serial Port Data Output. Serial data output for ASP interface. GPIO4. General-purpose input/output.	Programmable (pull-up, pull-down)	Output, passive pull down
ASP1_FSYNC/GPIO5	6	VDD_IO	I/O	Audio Serial Port Frame Sync. Frame sync for ASP interface. Optional clock source for PLL. GPIO5. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
GPIO13	15	VDD_IO	I/O	GPIO13. General-purpose input/output. MCLK. External clock reference input. WAKE. External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
INT	16	VDD_IO	I/O	Interrupt. Programmable open-drain interrupt output.	Programmable (pull-up, pull-down)	Output, Hi-Z
RESET	20	See Note 1	I	Reset. Active-low reset input.	—	Input
SPI1_MISO/I2C1_SCL/GPIO7	11	VDD_IO	I/O	SPI Control-Port Master In Slave Out. SPI data input. I2C Control-Port Clock. Clock input for the I2C interface. GPIO7. General-purpose input/output. WAKE. External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
SPI1_MOSI/I2C1_SDA/GPIO8	12	VDD_IO	I/O	SPI Control-Port Master Out Slave In. SPI data output. I2C Control-Port Data. Data input/output for the I2C interface. GPIO8. General-purpose input/output. WAKE. External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Output, Hi-Z
SPI1_SCK/GPIO9	8	VDD_IO	I/O	SPI Control-Port Clock. Clock input for the SPI interface. GPIO9. General-purpose output.	Programmable (pull-up, pull-down)	Input, passive pull down
SPI1_SS/GPIO10	9	VDD_IO	I/O	SPI Control-Port Slave Select. Active-low Slave Select input for the SPI interface. GPIO10. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, Hi-Z
GPIO11	13	VDD_IO	I/O	GPIO11. General-purpose input/output. MCLK. External clock reference input. WAKE. External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
GPIO12	14	VDD_IO	I/O	GPIO12. General-purpose input/output. WAKE. External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
SYNC/GPIO1	3	VDD_IO	I/O	Multidevice Synchronization. Serial data bus connecting devices in multi-channel applications. GPIO1. General-purpose input/output. MCLK. External clock reference input.	Programmable (pull-up, pull-down)	Input, passive pull down
Analog I/O						
ADDR	19	VDD_A	I	I2C Address Input. Address pin for I2C Target address. Latched on POR or hard reset.	—	—
BST_SW	34	—	I	Boost Switch. Input to internal boost FETs.	—	—
LDO_A_FILT	23	VDD_P	O	LDO_A Output. Decoupling point for analog supply (if powered from internal LDO).	—	—

Table 1-1. QFN Pin Descriptions (Cont.)

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
LDO_D_FILT	21	VDD_A	O	LDO_D Output. Decoupling point for digital supply, powered from LDO_D.	—	—
OUTN	30	VDD_AMP	O	Differential Output. Internal Class D amplifier output.	—	—
OUTP	29	VDD_AMP	O	Differential Output. Internal Class D amplifier output.	—	—
VBST	32	—	O	Boosted Supply from Boost Converter. Internal boost converter output.	—	—
VMON_N	27	VDD_AMP	I	Output Monitor. Voltage-sense input for OUTN. Must be connected to OUTN via 4.99 k Ω (1%) resistor.	—	—
VMON_P	26	VDD_AMP	I	Output Monitor. Voltage-sense input for OUTP. Must be connected to OUTP via 4.99 k Ω (1%) resistor.	—	—
Power Supplies						
GND	17, 18, 25	—	—	Note: Analog and Digital Ground. Ground return for the analog and digital functional blocks throughout the device.	—	—
GND_AMP	28	—	—	Power Ground. Ground reference for the Class D amplifier output stage.	—	—
GND_BST	1	—	—	Boost Converter Power Ground. Ground reference for the boost converter.	—	—
SUB_BST	33, PAD	—	—	Boost Substrate Ground and Thermal Pad. The thermal pad must be connected to ground.	—	—
VDD_A	22	—	I	Analog Supply. Power supply for the internal analog circuits. Also powers digital circuits via internal regulator.	—	—
VDD_P	24	—	I	System Supply. Power supply for always-on (Hibernate) circuits. Also powers the LDO_A regulator, which can be used to generate the VDD_A supply.	—	—
VDD_AMP	31	—	I	Amplifier Supply. Power supply for the Class D amplifier.	—	—
VDD_B	2	—	I	Boost Supply. Power supply for boost converter. (Note this is primarily a monitor pin; the boost current is conducted via the inductor to BST_SW.)	—	—
VDD_IO	10	—	I	Digital I/O Supply. Power supply for digital input/output.	—	—

1.5 V-tolerant input, supply-independent

2 Typical Connection Diagram

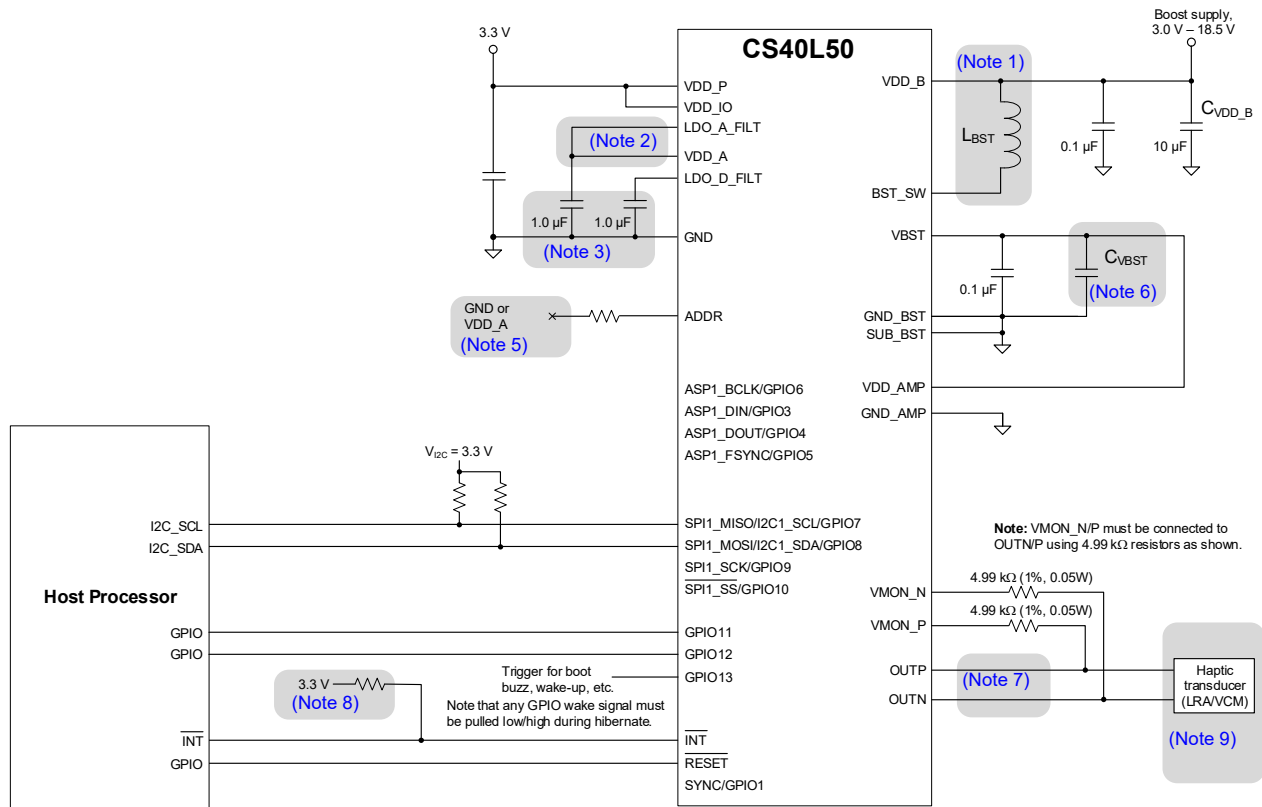


Figure 2-1. Typical configuration with internal boost power source

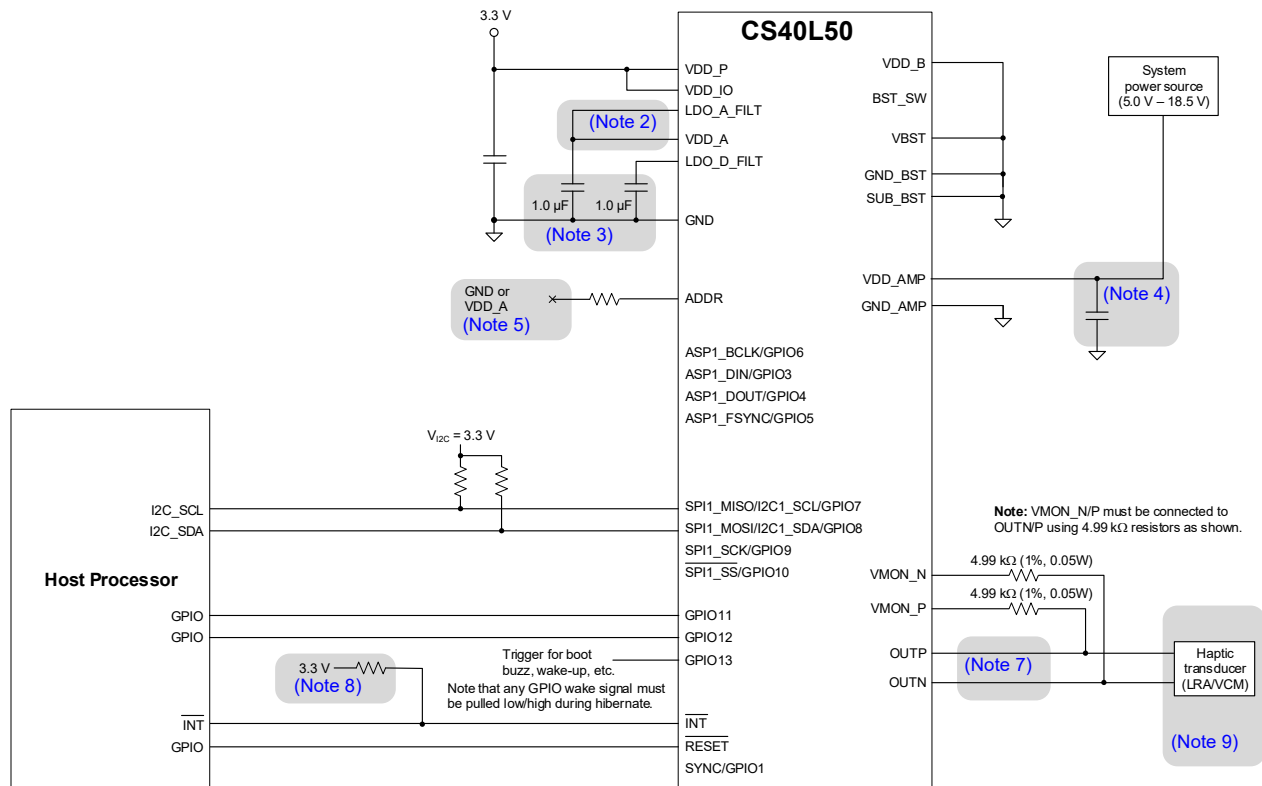


Figure 2-2. Typical configuration with external amplifier power source

Notes referenced in the typical connection diagrams:

1. The L_{BST} inductor must not derate to a value less than 0.5 μH . Inductance of 1.0 μH is recommended for typical applications.
2. In the configuration shown, the LDO_A regulator is used to generate the analog supply. The VDD_A supply pin is connected to the LDO output, LDO_A_FILT.
3. The LDO_A_FILT capacitor must not de-rate to a value less than 500 nF at 1.8 V. The LDO_D_FILT capacitor must not de-rate to a value less than 390 nF at 1.25 V.
4. The C_{VDD_AMP} capacitor must not derate to a value less than 2 μF at 18.5 V.
5. The I²C device address are configured using a resistor connected between the ADDR pin and GND, or else between the ADDR pin and VDD_A. The capacitive loading on the ADDR pin must not exceed 100 pF.
6. The C_{VBST} capacitor must not derate to a value less than 2 μF at 18.5 V.
7. Optional EMI-suppression capacitors between OUTx and GND_AMP may be used, depending on the application requirements. The capacitance should not exceed 470 pF, as higher capacitance increases switching losses.
8. In the configuration shown, the CS40L50 $\overline{\text{INT}}$ pin is configured as an open-drain output and an external pull-up resistor (e.g., 100 k Ω) to VDD_IO is required.
9. When using a simulated load of 8 Ω + 33 μH , a Coilcraft DO5040H–333MLB inductor is used.

General notes and recommendations:

- [Fig. 2-1](#) through [Fig. 2-2](#) are examples intended to describe the connectivity of each functional block within the CS40L50, and do not limit all possible use cases.
- All external passive component values listed are nominal values.

3 Characteristics and Specifications

Note: The default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_AMP = GND_BST = 0 V; voltages are with respect to ground.

Parameter ¹		Symbol	Minimum	Maximum	Unit	
DC power supply	Analog and digital supply	VDD_P	3.0	5.5	V	
	Digital I/O supply	VDD_IO	1.71	3.6	V	
	Analog supply ²	VDD_A	1.71	1.89	V	
	Boost converter ^{3, 4}	VDD_B	3.0	18.5	V	
	Amplifier supply ⁵	VDD_AMP	5.0	18.5	V	
Supply ramp up/down		VDD_P, VDD_IO, VDD_A VDD_B, VDD_AMP	tPWR-UD	0.1 0.2	100 100	ms ms
External voltage applied to digital input/output		VDD_IO input/output pins ⁶ RESET pin	V _{INDI}	–0.3 –0.3	VDD_IO + 0.3 5.5	V V
External voltage applied to analog inputs		ADDR pin	V _{INAI}	–0.3	VDD_A + 0.3	V
External voltage applied to analog inputs		VMON_x pins	V _{IN-VMON}	–0.3	VDD_AMP + 0.3	V
External voltage applied to analog outputs		OUTP, OUTN pins	V _{IN-OUTx}	–0.3	VDD_AMP + 0.3	V
Ambient temperature		T _A	–40	+85		°C

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. There are no sequencing requirements associated with any of the supplies—each can be enabled or removed independently of the other supplies.
2. The analog supply can be generated by the internal LDO (powered from VDD_P), or else provided externally. If the LDO is used, the VDD_A pin must be connected to the LDO output pin (LDO_A_FILT) and must not be connected to any external supply.
3. Note VDD_B is the voltage-monitor point for the boost converter; the load current path is through the inductor to the BST_SW.
4. If the amplifier is powered directly using an external supply to VDD_AMP, the VDD_B supply is not required.
5. The amplifier supply can be generated by the boost converter, or else provided externally. If the boost converter is used, the VDD_AMP pin must be connected to the boost-converter output pin, VBST.
6. All digital I/O pins except RESET.

Table 3-2. Absolute Maximum Ratings

Test conditions (unless specified otherwise): Ground = GND = GND_AMP = GND_BST = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog and digital supply	VDD_P	–0.3	6	V
	Digital I/O supply	VDD_IO	–0.3	4.32	V
	Analog supply	VDD_A	–0.3	2.27	V
	Boost converter	VDD_B	–0.3	22	V
	Amplifier supply	VDD_AMP	VDD_B – 0.3	22	V
Input current	digital I/O (per pin)	I _{in}	—	±10	mA
	ADDR pin		—	±10	mA
Output load impedance		Z _{L1}	3	—	Ω
Ambient operating temperature (local to device, power applied)		T _A	–50	+115	°C
Junction operating temperature (power applied)		T _J	–40	+150	°C
Storage temperature		T _{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Table 3-1](#), is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4 Package Dimensions

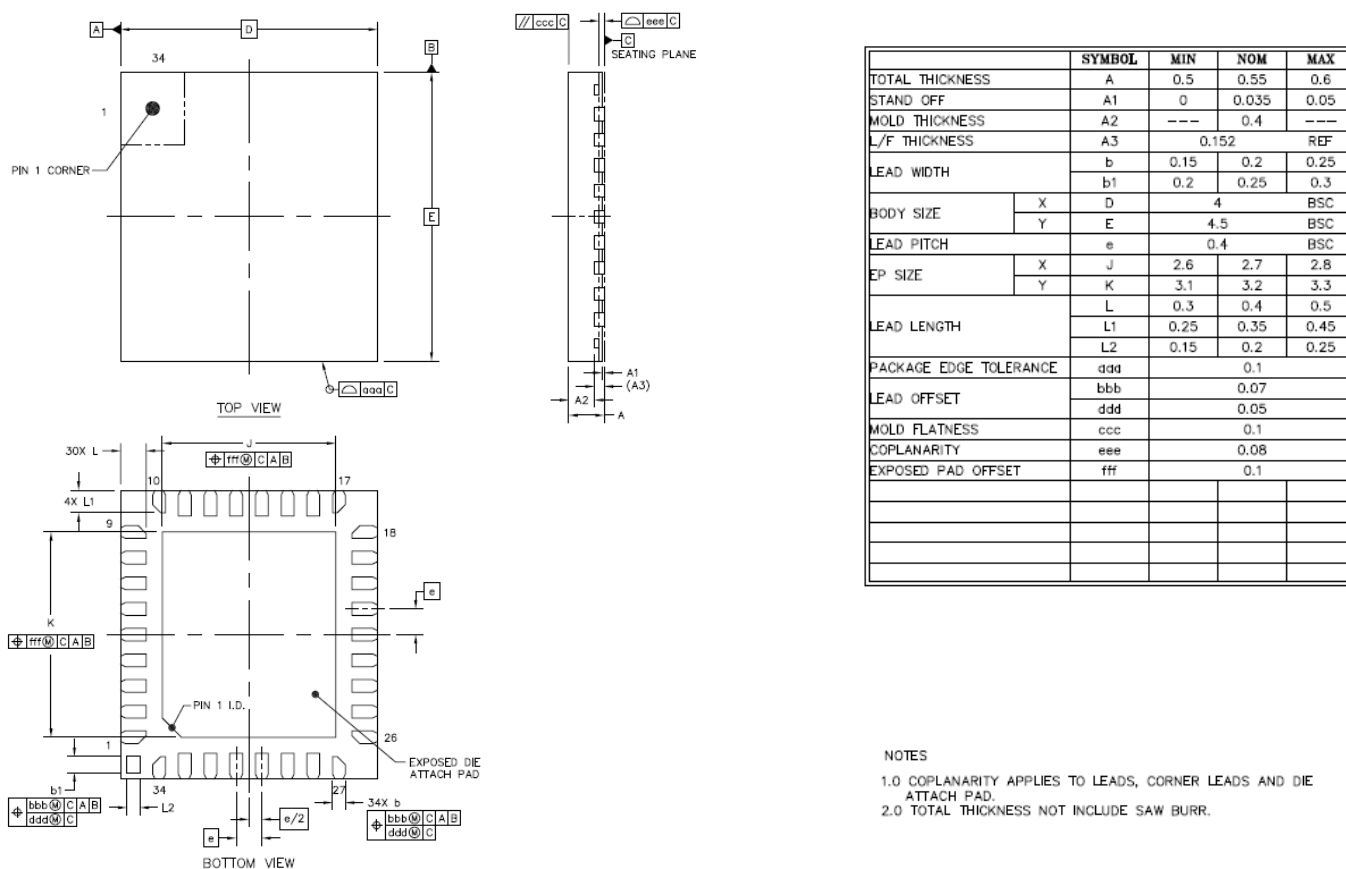


Figure 4-1. QFN Package Drawing

5 Package Marking

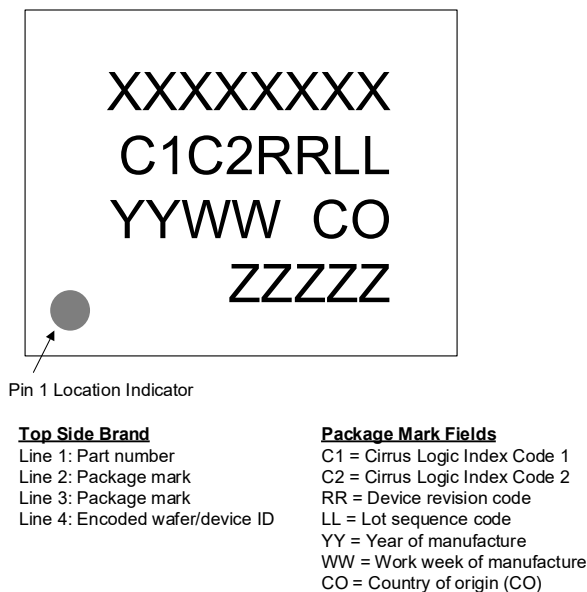


Figure 5-1. Package Marking

6 Ordering Information

Table 6-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS40L50	Advanced Haptic Driver with Waveform Memory, Integrated DSP, and Closed-Loop Algorithms	34-pin QFN	Yes	Commercial	–40 to +85°C	Tape and Reel	CS40L50–CNR

7 Revision History

Table 7-1. Revision History

Revision	Changes
R1 JUN 2024	Initial version

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

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