

PC Smart Amplifier with Speaker Protection and Audio Enhancement Algorithms

Features

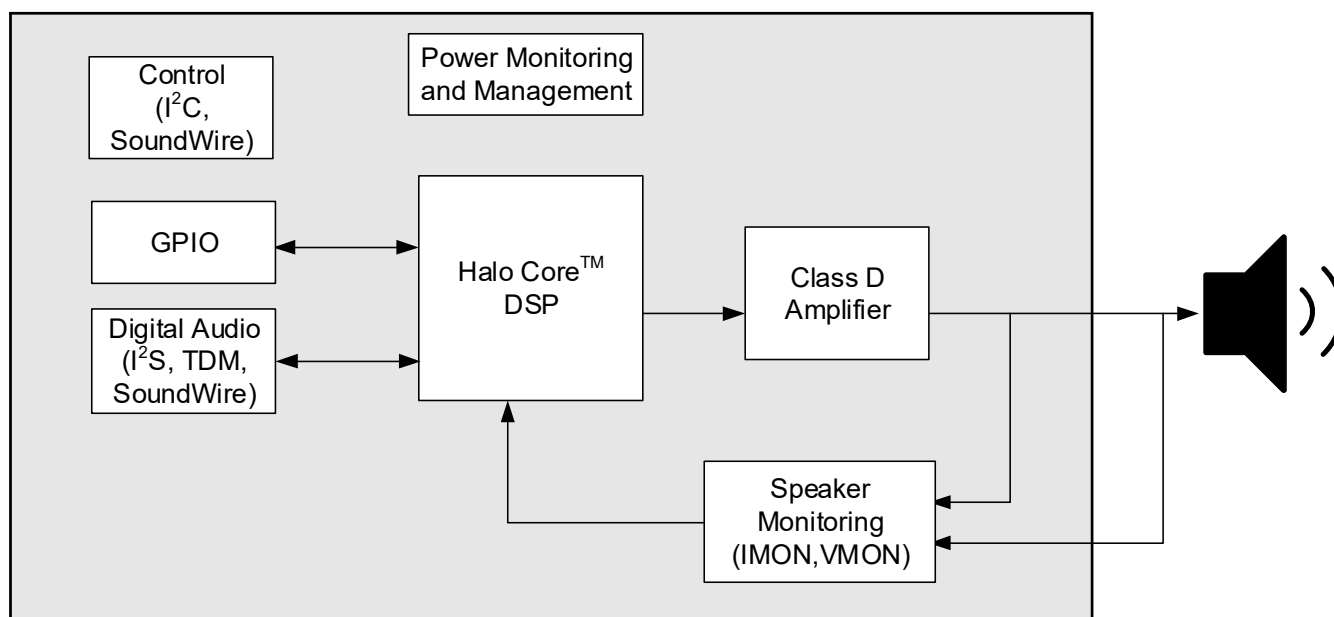
- **Mono Class-D Amplifier:** minimizes power consumption and switching losses
- **Up to 15 V amplifier supply:** supports multicell 2S or 3S systems directly from the battery
- **130 MCPS Halo Core™ DSP:** on-chip speaker protection and audio enhancement algorithms
- **Speaker current and voltage sensing:** on-chip speaker excursion and thermal protection
- **SoundWire support:** SDCA v1.0 and SoundWire v1.2.1 conformant with multi-lane support
- **Legacy interfaces:** I2S and I2C interface ports
- **Streamlined system integration:** AEC reference, boot beep, ultrasonic output, digital I/O, and power-sequencing implementations

Specifications

- Output into 4 Ω load, VDD_AMP = 12.6 V:
 - 14.8 W @ 1% THD+N
- Output into 8 Ω load, VDD_AMP = 12.6 V:
 - 8.8 W @ 1% THD+N
- 0.015% THD+N @ 1 W for high-fidelity audio
- 5.0 V–15 V Class D amplifier supply
- 15 mW quiescent power in Idle (VDD_AMP = 12.6 V, noise gate enabled)
- 5.45 mm² WLCSP package supporting Type-III PCB routing requirements

Applications

- Notebooks and ultrabooks
- 2-in-1 and detachable PCs



Monitoring Features

- Speaker current monitoring via integrated sense circuit
- Current and voltage monitor data feedback for AEC reference or other functions

Efficiency and Power Consumption

- 131 μ W power consumption in hibernate (RAM contents retained, monitoring for I²C or activity on GPIO pins)
- 15 mW quiescent idle power consumption with LDPM, all monitoring disabled, and noise gate enabled

Halo Core DSP

- Speaker excursion protection and thermal protection
- Speaker equalization and enhancement
- Signal clipping prevention
- Posture-aware seamless switching (PASS) enables alternate speaker tuning based on orientation or hinge-angle rotation
- Firmware support for audio sample rates 48 kHz and 96 kHz
- Ultrasonic signal output concurrent with audio playback

System Hardware Protection Features

- IC thermal self-protection
- Amplifier supply voltage monitoring
- Amplifier short-circuit protection

System Integration Features

- Boot beep waveform stored on chip, triggered by GPIO without any driver/OS intervention, I²C interface, or via SoundWire
- Support for Pulse Frequency Modulation (PFM) input for boot beep
- Ultrasonic output: flexible signal architecture options
- Support for 1.8 V with BEEP/GPIO8, MUTE/GPIO9, MDSYNC/ $\overline{\text{IRQ}}$ /GPIO1, GPIO2, and GPIO4 functions supporting up to 3.3 V input overdrive eliminating the need for level shifters

Clocking and Data Interface Features

- Digital audio input over I²S/TDM/SoundWire interfaces
- Clocks generated from audio serial port or SoundWire interface using internal phase-locked loop (PLL)
- Open-loop PLL mode for autonomous tone/waveform playback with no external clock required
- Dual-mode audio/data serial port (ASP)
 - I²S and TDM interface formats
 - Tristate data output pin supports multi-device bus sharing
 - Support for 1.8 V signals
- SoundWire peripheral interface
 - MIPI® SoundWire version 1.2.1 conformant
 - Implements SDCA smart-amp function
 - Up to 8 unique addressable instances
 - Support for 1.8 V signals
 - Supports 2 data lanes
- I²C control port
 - Supports Standard-mode (Sm), Fast-mode (Fm), Fast-mode Plus (Fm+), and High-speed mode (Hs-mode) operation
 - Up to 8 unique I²C target address instances
 - Supports I²C broadcast address to enable simultaneous code download to multiple devices
- Multidevice synchronization (MDSYNC)
 - Communication of device power-up and protection events for up to 8 devices
- Programmable and maskable interrupts with hardware interrupt pin (push-pull/open-drain) and software polling
- 4 GPIO pins with multiple features for Type III PCB boards
 - Optional external reference clock (MCLK) support from 32 kHz to 24.576 MHz
 - Device power up/down transitions
 - Hardware mute
 - I²C optionally provides 2 GPIO pins
 - Native 1.8 V I/O with 3.3 V tolerant input
- I²S or 3 additional GPIOs for High-Density Interconnect (HDI) PCBs

General Description

The CS35L63 combines a high-performance mono audio amplifier with a Halo Core DSP to enable an easy-to-integrate smart amplifier solution.

The CS35L63 is an impressively small PC smart amplifier with a total footprint of less than 35 mm², including external BOM components. Combining a high-performance Class D amplifier with a 130 MCPS DSP in a compact 5.45 mm² Type-III PCB compatible package enables an easy-to-integrate, smart amplifier solution to be placed almost anywhere on a PCB. This can minimize high-power analog switching traces, improving noise performance and saving further PCB area.

The Class D amplifier supports supply voltages up to 15 V. The amplifier incorporates an advanced closed-loop architecture and a complementary output stage capable of driving up to 14.8 W into a 4 Ω load at 1% THD+N. The amplifier can be powered by multicell 2S or 3S batteries, reducing the need for external DC-DC converters. This, in turn, lowers BOM cost, decreases size, and increases system power efficiency.

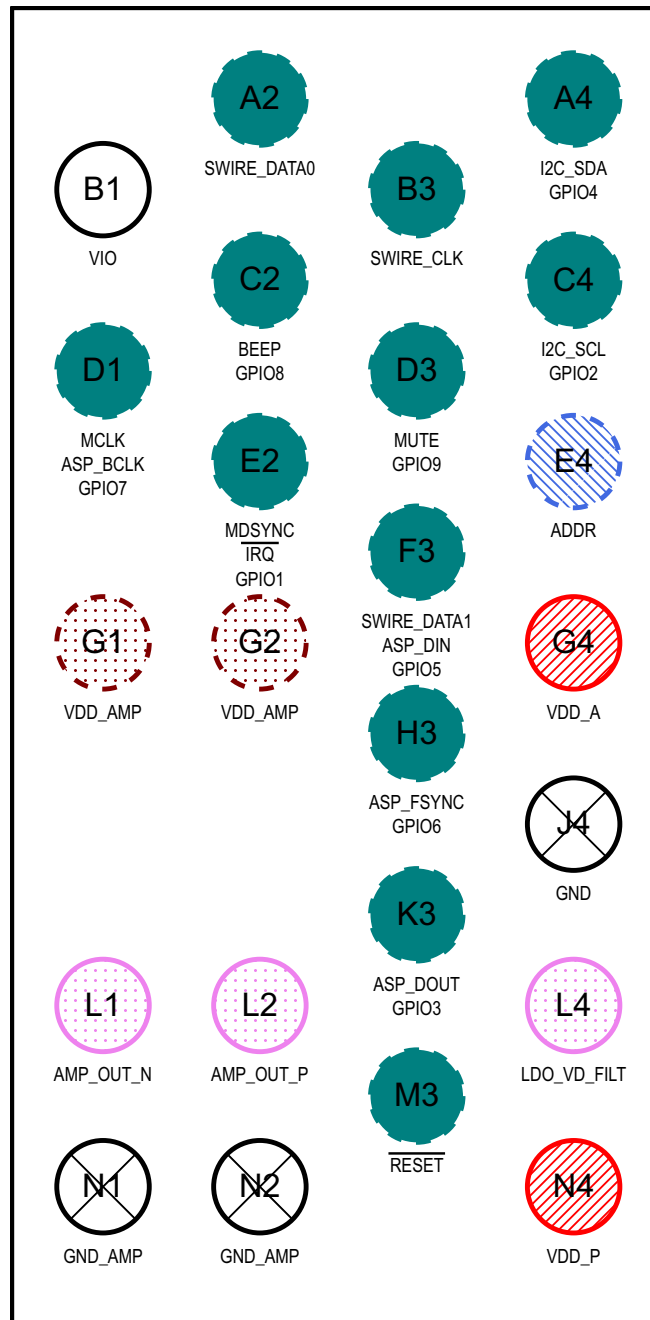
The integrated DSP provides speaker protection, audio enhancement, and power-management functions, offloading some tasks from the host processor. Excursion and thermal-protection algorithms can be tailored to the back volume, porting, and acoustics of the speaker to transparently maximize acoustic output. The enhancement algorithms provide comprehensive capability to fine tune the desired audio characteristics. Cirrus Logic provides an optimized tool chain to create and program the audio-enhancement and speaker-protection coefficients for development and mass production.

The CS35L63 offers numerous features to ease system integration. The SoundWire interface (v1.2.1 and SDCA 1.0 conformant) enables simple integration with a SDCA host. I²S and I²C legacy interfaces are also supported for other architectures. Additional features such as boot-beep, ultrasonic output, and AEC reference-signal aggregation are supported on-chip for further offloading from the host processor and simpler integration.

The CS35L63 is available in a commercial-grade 24-pin WLCSP package for operation from –40° to +85°C.

1 Pin Assignments and Descriptions

1.1 WLCSP Pin Out (Top View, Through-Package)



Not to scale



Figure 1-1. WLCSP Staggered Array 24-Pin Diagram (Top View, Through-Package)

1.2 WLCSP Pin Descriptions

Table 1-1. WLCSP Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
ADDR	E4	VDD_A	I	I²C Address/SoundWire ID Detect. Address pin for I ² C Target address and SoundWire UNIQUE_ID instance number determination. Latched on POR or RESET.	—	—
AMP_OUT_N	L1	VDD_AMP	O	Differential Negative Output. Internal Class D amplifier negative output.	—	—
AMP_OUT_P	L2	VDD_AMP	O	Differential Positive Output. Internal Class D amplifier positive output.	—	—
ASP_DOUT/ GPIO3	K3	VIO	I/O	Audio Serial Port Data Output. Serial data output for two's complement serial PCM audio data. GPIO3. General-purpose input/output.	Programmable (weak pull up/ pull down)	Hi-Z
ASP_FSYNC/ GPIO6	H3	VIO	I/O	Audio Serial Port Frame Sync Clock. Identifies the start of each serialized PCM data word and indicates the start of each TDM frame. GPIO6. General-purpose input/output.	Programmable (weak pull up/ pull down)	Weak pull down
BEEP/GPIO8	C2	VDD_A	I/O	Beep trigger/signal input. Input trigger to generate a beep output, or input to decode a PFM input signal to generate a beep output. Functional in all states except when configured for GPIO function. GPIO8. General-purpose input/output.	Programmable (weak pull up/ pull down)	Weak pull down
GND	J4	—	—	Analog and Digital Ground. Ground return for the analog and digital functional blocks throughout the device.	—	—
GND_AMP	N1, N2	—	—	Power Ground. Ground return for the Class D amplifier output stage.	—	—
I2C_SCL/GPIO2	C4	VDD_A	I/O	I²C Control-Port Clock. Target port clock input for the I ² C interface. GPIO2. General-purpose input/output.	Hi-Z, Programmable (weak pull up/ pull down)	Hi-Z
I2C_SDA/GPIO4	A4	VDD_A	I/O	I²C Control-Port Data. Target port data input/output for the I ² C interface. GPIO4. General-purpose input/output.	Hi-Z, Programmable (weak pull up/ pull down)	Hi-Z
LDO_VD_FILT	L4	VDD_A	O	LDO_D Output. Decoupling point for digital supply, powered from LDO_D.	—	—
MCLK/ASP_ BCLK/GPIO7	D1	VIO	I/O	Main clock input. Audio Serial Port Bit Clock. Serial shift clock for ASP interface. GPIO7. General-purpose input/output. Can be also configured for use as a MCLK input.	Programmable (weak pull up/ pull down)	Weak pull down
MDSYNC/ $\overline{\text{IRQ}}$ / GPIO1	E2	VDD_A	I/O	Multidevice Synchronization. Serial data bus connecting devices in multi-channel applications. Interrupt Request. Programmable, open-drain, active-low programmable interrupt output. GPIO1. General-purpose input/output. By default MDSYNC/ $\overline{\text{IRQ}}$ /GPIO1 is configured for bus keeper operation and should be reconfigured when using IRQ or GPIO functionality.	Programmable (bus keeper, weak pull up/ pull down)	Weak pull down

Table 1-1. WLCSP Pin Descriptions (Cont.)

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
MUTE/GPIO9	D3	VDD_A	I/O	Mute. When asserted, the amplifier output will be muted. GPIO9. General-purpose input/output.	Programmable (weak pull up/pull down)	Weak pull down
RESET	M3	See Note 1	I	Reset. The device enters a low power mode when this pin is driven low. RESET must be driven according to its VIH/VIL.	—	Hi-Z
SWIRE_CLK	B3	VIO	I	SoundWire Serial Clock. Clock input for the SoundWire peripheral interface.	—	Hi-Z
SWIRE_DATA0	A2	VIO	I/O	SoundWire Serial Data Lane 0. Serial data input/output for the SoundWire peripheral interface.	—	Hi-Z
SWIRE_DATA1/ ASP_DIN/GPIO5	F3	VIO	I/O	SoundWire Serial Data Lane 1. Serial data input/output for the SoundWire peripheral interface. Audio Serial Port Data Input. Serial data input for two's complement serial PCM audio data. GPIO5. General-purpose input/output.	Hi-Z, Programmable (weak pull up/pull down)	Hi-Z
VDD_A	G4	—	I	Analog Power Supply. Power supply for the internal analog circuits and non-SoundWire and ASP pins. Also powers digital circuits via internal regulator.	—	—
VDD_AMP	G1, G2	—	I	Amplifier Power Supply. Power supply for Class D amplifier.	—	—
VDD_P	N4	—	I	System Supply. Power supply for the always-on (Hibernate) circuitry and portions of the Class D amplifier's controller.	—	—
VIO	B1	—	I	Digital I/O Supply. Power supply for SoundWire and Audio Serial Port (ASP) digital input/output pins.	—	—

1. Supply-independent 5 V-tolerant input.

1.3 Termination of Unused Pins

Some systems may not need to connect to all of the IC pins. [Table 1-2](#) shows the recommended termination for any permanently unused pins. Pins not listed must be connected as shown in the typical connection drawings (see [Section 2](#)). A pin that is connected to other circuits but is only occasionally active is not required to follow the terminations shown.

Table 1-2. Termination of Unused Pins

Name	Termination if Unused
MCLK/ASP_BCLK/GPIO7 ASP_FSYNC/GPIO6 BEEP/GPIO8 MUTE/GPIO9	Float or connect to GND
ADDR MDSYNC/IRQ/GPIO1 I2C_SCL/GPIO2 I2C_SDA/GPIO4 SWIRE_CLK SWIRE_DATA0 SWIRE_DATA1/ASP_DIN/GPIO5 ASP_DOUT/GPIO3	Connect to GND
RESET	Pull up to VDD_A or VDD_P

1.4 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS35L63 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to JEDEC ESD protection standards.

2 Typical Connection Diagram

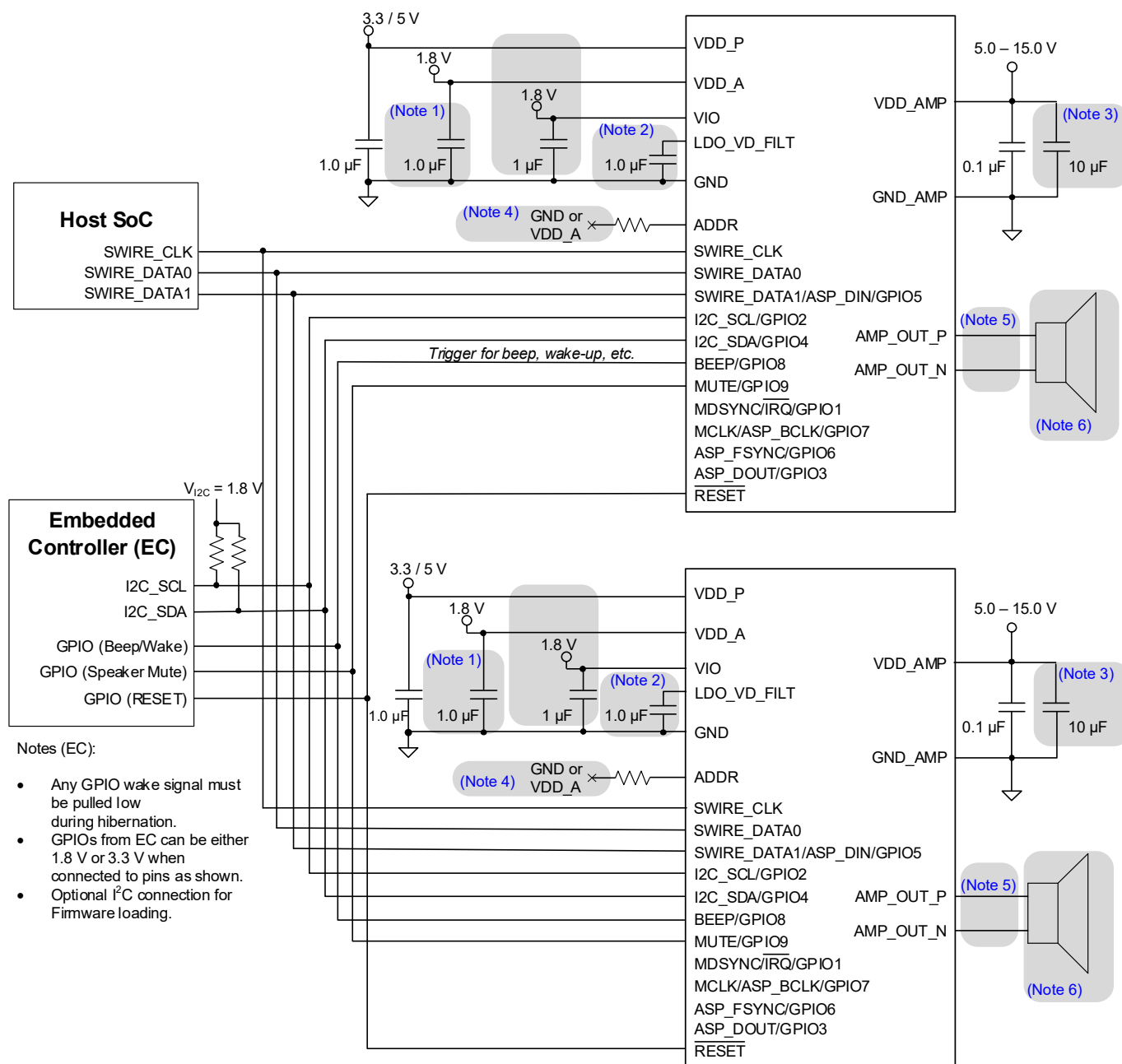


Figure 2-1. Stereo Configuration with SoundWire control

Notes referenced in the typical connection diagrams:

1. The VDD_A capacitor must not de-rate to a value less than 500 nF at 1.8 V.
2. The LDO_VD_FILT capacitor must not de-rate to a value less than 390 nF at 1.25 V and a value no more than 10 µF. Additionally, it is recommended to not exceed a total of 150 mΩ ESR and 1 nH ESL on this pin.
3. The C_{VDD_AMP} capacitor must not derate to a value less than 2 µF at 15 V.
4. The I²C device address and SoundWire unique instance ID are configured using a resistor connected between the ADDR pin and GND, or else between the ADDR pin and VDD_A. The capacitive loading on the ADDR pin must not exceed 100 pF.

5. Optional EMI-suppression capacitors between AMP_OUT_x and GND_AMP may be used, depending on the application requirements. The capacitance should not exceed 470 pF, as higher capacitance increases switching losses.
6. When using a simulated load of $8\ \Omega + 33\ \mu\text{H}$, a Coilcraft DO5040H–333MLB inductor is used.

General notes and recommendations:

- [Fig. 2-1](#) is intended to describe the connectivity of each functional block within the CS35L63 and does not limit all possible use cases.
- All external passive component values listed are nominal values.

3 Characteristics and Specifications

Note: The default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Recommended Operating Conditions

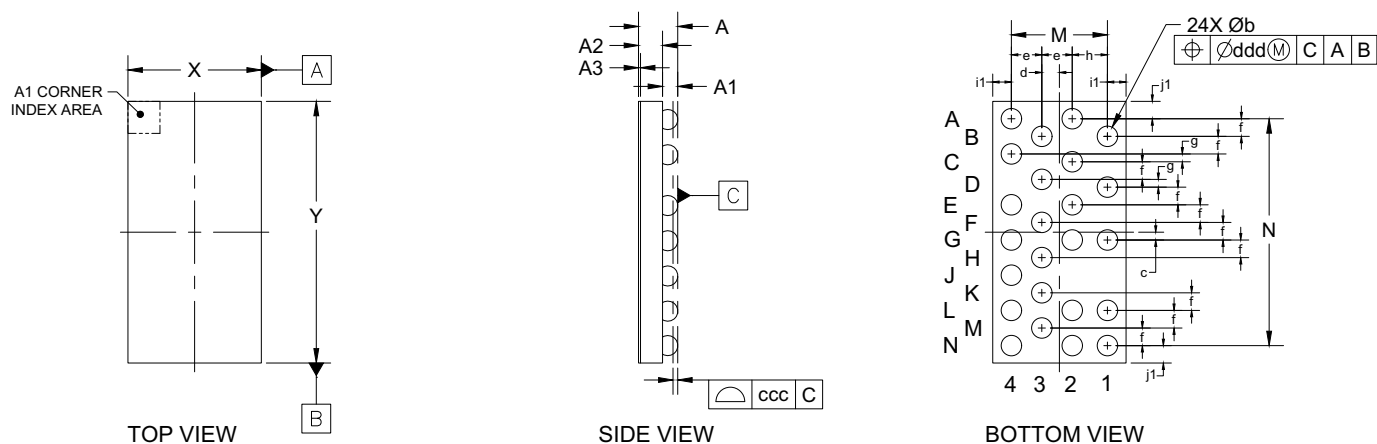
Test conditions (unless specified otherwise): Ground = GND = GND_AMP = 0 V; voltages are with respect to ground.

Parameter ¹		Symbol	Minimum	Maximum	Unit	
DC power supply	Analog and digital supply	VDD_P	3.0	5.5	V	
	Analog supply	VDD_A	1.71	1.89	V	
	Amplifier supply	VDD_AMP	5.0	15.0	V	
	SoundWire and ASP I/O, 1.8 V nominal	VIO	1.7	1.9	V	
Supply ramp up/down		VDD_P, VDD_A, VIO VDD_AMP	tPWR-UD 0.1 0.2	100 100	ms ms	
External voltage applied to digital input/output		RESET pin I ² C, BEEP, MUTE, IRQ pins ² SWIRE_x and ASP pins	VINDI -0.3 -0.3 -0.3	5.5 3.6 VIO + 0.3	V V V	
External voltage applied to analog inputs		ADDR pin	VINAI	-0.3	VDD_A + 0.3	V
External voltage applied to analog outputs		AMP_OUT_x pins	VIN-OUTx	-0.3	VDD_AMP + 0.3	V
Ambient temperature		T _A	-40	+85	°C	

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. There are no sequencing requirements associated with any of the supplies—each can be enabled or removed independently of the other supplies.
2. Applies to all associated GPIO pins.

4 Package Dimensions



Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.46	0.49	0.52
A1	0.175	0.19	0.205
A2	0.285	0.3	0.315
A3	REF	0.025	REF
b	0.235	0.255	0.275
c	0.09	0.0975	0.105
d	0.2125	0.22	0.2275
e	BSC	0.38	BSC
f	REF	0.22	REF
g	REF	0.0975	REF
h	REF	0.44	REF
i1	REF	0.2333	REF
j1	REF	0.2177	REF
M	BSC	1.2	BSC
N	BSC	2.835	BSC
X	1.6416	1.6666	1.6916
Y	3.2454	3.2704	3.2954
ccc=0.03			
ddd=0.015			

Notes: Controlling dimension is millimeters.

Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C. X/Y Tolerances can apply to an individual edge increasing or decreasing by 25µm.

Figure 4-1. WLCSP Package Drawing

5 Ordering Information

Table 5-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS35L63	PC Smart Amplifier with Speaker Protection and Audio Enhancement Algorithms	24-pin WLCSP	Yes	Commercial	–40 to +85°C	Tape and Reel	CS35L63-DWR

6 References

- NXP Semiconductors, UM10204 Rev. 7.0, October 2021, *I2C-Bus Specification and User Manual*, <https://www.nxp.com>
- MIPI Alliance Version 1.2.1, June 2021, *MIPI SoundWire Specification*, <https://www.mipi.org/>
- MIPI Alliance, Version 1.0, October 2023, *Specification for SoundWire Device Class for Audio (MIPI SDCA)*, <https://www.mipi.org/>

Contacting Cirrus Logic Support

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