

18.5 V Class D Smart Amplifier with Multi-Cell Battery Boost

Features

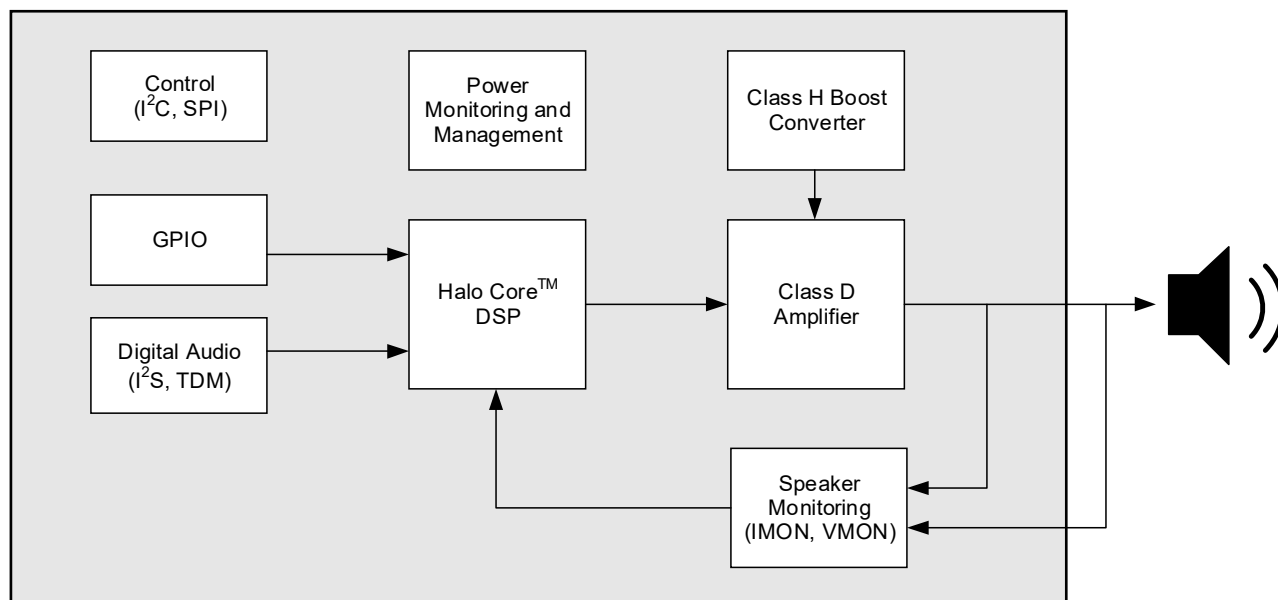
- **Multi-cell battery boost:** up to 15 V output from 2S, 3S, or 4S batteries, for maximum speaker output and consistent performance across battery conditions
- **Up to 18.5 V amplifier supply:** Class D amplifier can be powered externally (boost converter disabled)
- **130 MCPS Halo Core™ DSP:** on-chip speaker protection and audio enhancement algorithms
- **Speaker current and voltage sensing:** on-chip speaker excursion and thermal protection
- **SoundWire support:** SDCA and SoundWire v1.2 conformant
- **Legacy interfaces:** I²S, I²C and SPI ports
- **Streamlined system integration:** simple AEC reference, boot beep, ultrasonic output, digital I/O, and power-sequencing implementations

Specifications

- 14.0 W @ 1% THD+N (4 Ω, 12.6 V, external supply)
- 9.5 W @ 1% THD+N (8 Ω, 8.4 V, internal boost)
- 5.0 V–18.5 V Class D amplifier supply
- 15 V internal boost output
- 3.0 V–18.5 V internal boost supply
- 85% device efficiency @ 1 W output
- 9 mW quiescent power in Idle
- 44 μW power consumption in Hibernate State
- 31-ball CSP package, 0.43 mm pitch
- 2.79 × 2.6 mm package size

Applications

- Notebooks and ultrabooks
- 2-in-1 and detachable PCs



Speaker Amplifier Features

- Class D architecture minimizes idle power consumption and switching losses
- Amplifier supply voltage up to 18.5 V
- –77 dB THD+N @ 1 W into 8 Ω

Monitoring Features

- Speaker current and voltage monitoring
- Current and voltage monitor data feedback over I²S/TDM/SoundWire interface for AEC reference or other functions

Efficiency and Power Consumption

- 85% overall efficiency at 1.0 W output (8 Ω load, 8.4 V internal boost)
- 44 μ W power consumption in hibernate (RAM contents retained, monitoring for I²C or activity on GPIO/SPI pins)
- 7 mW quiescent idle power consumption with LDPM, Class H enabled, and all monitoring disabled

Halo Core™ DSP

- Speaker excursion protection and thermal protection
- Speaker equalization and enhancement
- Signal clipping prevention
- Posture-aware seamless switching (PASS) enables alternate speaker tuning based on orientation or hinge-angle rotation
- Firmware support for audio sample rates 48 kHz and 96 kHz
- Ultrasonic signal output concurrent with audio playback

System Hardware Protection Features

- IC thermal self-protection
- Boost battery-brownout protection engine (BPE)
- Boost converter overvoltage/undervoltage protection
- Boost/amplifier short-circuit protection

Digital Boost Converter Features

- Programmable boost output voltage up to 15 V
- Advanced boost Class-H engine tracks audio envelope to maximize power efficiency
- Programmable boost inductor current limits up to 4 A
- Integrated boost and rectification FETs

System Integration Features

- Boot beep waveform stored on chip, triggered by GPIO without any driver/OS intervention
- AEC reference-signal aggregation from up to eight amplifiers
- Ultrasonic output: flexible signal architecture options
- Support for 1.8 V and 3.3 V digital input/output

Clocking and Data Interface Features

- Digital audio input over I²S/TDM/SoundWire interfaces
- Clocks generated from audio serial port or SoundWire interface using internal phase-locked loop (PLL)
- Open-loop PLL mode for autonomous tone/waveform playback with no external clock required
- Dual-mode audio/data serial port (ASP)
 - I²S and TDM interface formats
 - Tristate data output pin supports multi-device bus sharing
- SoundWire peripheral interface
 - MIPI® SoundWire version 1.2 conformant
 - Implements SDCA smart-amp function
 - Up to eight unique addressable instances
- I²C control port
 - I²C High Speed, Fast-mode and Fast-mode Plus (Fm+) modes
 - Up to eight unique I²C target address instances
 - Supports I²C broadcast address to enable simultaneous code download to multiple devices
- SPI control port
 - SPI operation up to 17 MHz
- Multidevice synchronization (MDSYNC)
 - Communication of device power-up and protection events for up to eight devices
- Programmable and maskable interrupts with hardware interrupt pin (push-pull/open-drain) and software polling
- GPIO pins with multiple features
 - Optional external reference clock
 - Device power up/down transitions
 - Hardware trigger for beep waveform playback
 - Configurable by I²C, SPI, SoundWire, or by DSP core

General Description

The CS35L57 combines a high-performance mono audio amplifier, Class-H tracking inductive boost converter, and Halo Core™ DSP to enable an easy-to-integrate smart amplifier solution.

The Class D amplifier supports supply voltages up to 18.5 V. The amplifier incorporates an advanced closed-loop architecture and a complementary output stage capable of driving up to 14.0 W into a 4 Ω load at 1% THD+N.

The DC-DC boost converter supports Class-H tracking and generates up to 15 V output from a wide range of common battery supplies, maximizing speaker performance and maintaining a consistent listening experience across battery conditions. Using the internal-boost configuration, the CS35L57 delivers up to 5.9 W into a 8 Ω load at 1% THD+N. The boost converter can be powered by multicell 2S, 3S, and 4S batteries, reducing the need for external DC-DC converters and enabling the best possible BOM cost, size, and system-power efficiency.

The integrated DSP provides speaker protection, audio enhancement, and power-management functions, reducing the loading of the host processor. Excursion and thermal-protection algorithms can be tailored to the back volume, porting, and acoustics of the speaker to transparently maximize acoustic output. The enhancement algorithms provide comprehensive capability to fine tune the desired audio characteristics. Cirrus Logic provides an optimized tool chain to create and program the audio-enhancement and speaker-protection coefficients for development and mass production.

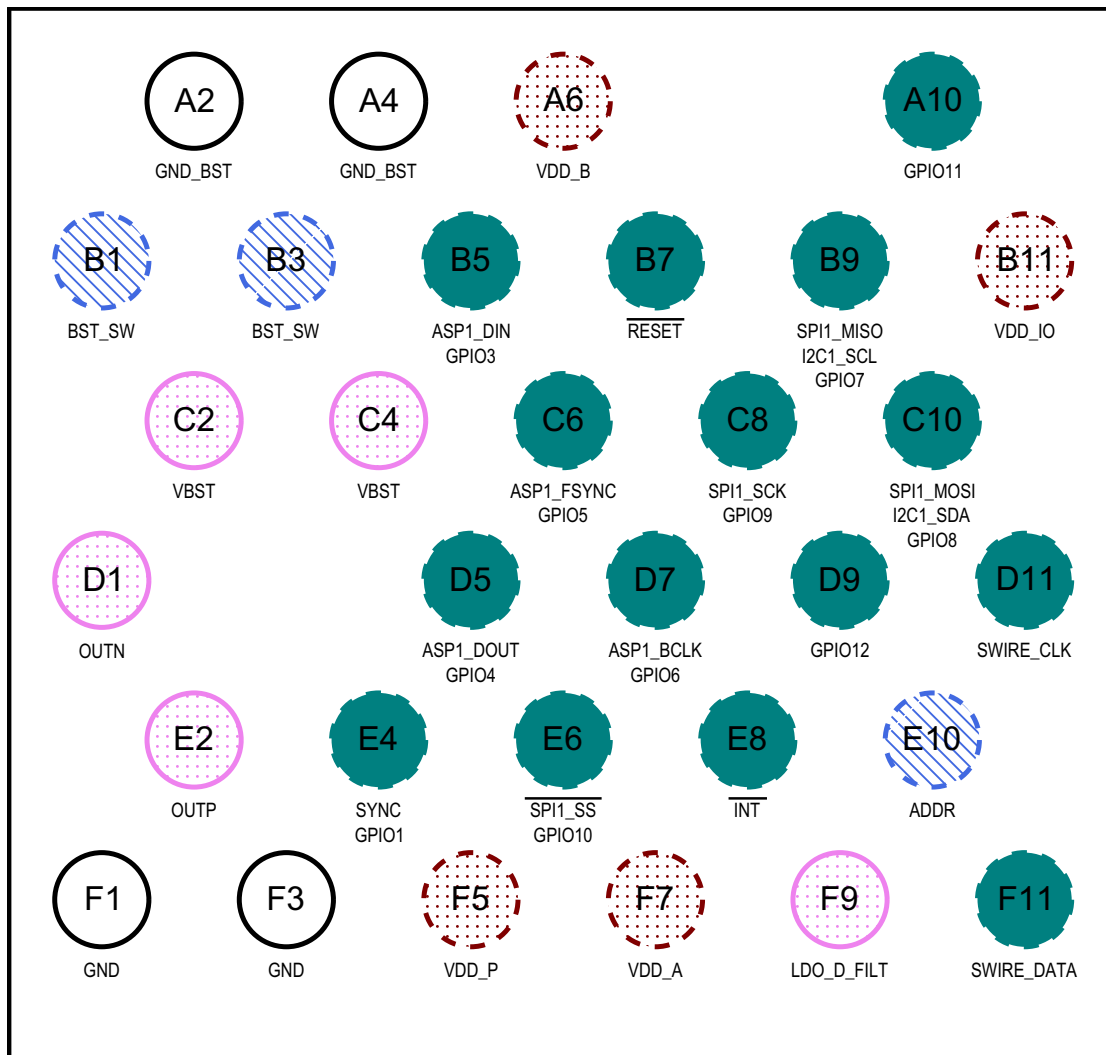
The CS35L57 offers numerous features to ease system integration. The SoundWire interface (v1.2 and SDCA conformant) enables simple integration with an SDCA host. Legacy interfaces including I²S, I²C, and SPI are also supported for other architectures including HDA. Additional features such as boot-beep, ultrasonic output, and AEC reference-signal aggregation are supported on-chip for further offloading from the host processor and simpler integration.

The CS35L57 is available in a commercial-grade 0.43 mm pitch, 31-ball CSP package for operation from –40° to +85°C.

See [Section 5](#) for ordering information.

1 Pin Assignments and Descriptions

1.1 31-Ball CSP (Top View, Through-Package)



Not to scale



Figure 1-1. CSP 31-ball diagram (Top View, Through Package)

Note: Some PCB designs may not support signal routing to the inner balls of the CSP individually, due to the reduced ball spacing. See [Section 1.3](#) for pin allocations supporting SoundWire applications that do not require access to these balls.

1.2 CSP Ball Descriptions

Table 1-1. CSP Ball Descriptions

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
Digital I/O						
ASP1_BCLK/GPIO6	D7	VDD_IO	I/O	Audio Serial Port Bit Clock. Serial shift clock for ASP interface. Optional clock reference for PLL. GPIO6. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
ASP1_DIN/GPIO3	B5	VDD_IO	I/O	Audio Serial Port Data Input. Serial data input for ASP interface. GPIO3. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
ASP1_DOUT/GPIO4	D5	VDD_IO	I/O	Audio Serial Port Data Output. Serial data output for ASP interface. GPIO4. General-purpose input/output.	Programmable (pull-up, pull-down)	Output, passive pull down
ASP1_FSYNC/GPIO5	C6	VDD_IO	I/O	Audio Serial Port Frame Sync. Frame sync for ASP interface. Optional clock source for PLL. GPIO5. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
GPIO11	A10	VDD_IO	I/O	GPIO11. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, Hi-Z
GPIO12	D9	VDD_IO	I/O	GPIO12. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, Hi-Z
$\overline{\text{INT}}$	E8	VDD_IO	I/O	Interrupt. Programmable open-drain interrupt output.	Programmable (pull-up, pull-down)	Output, Hi-Z
$\overline{\text{RESET}}$	B7	See Note 1	I	Reset. Active-low reset input.	—	Input
SPI1_MISO/I2C1_SCL/GPIO7	B9	VDD_IO	I/O	SPI Control-Port Master In Slave Out. SPI data output. I2C Control-Port Clock. Clock input for the I2C interface. GPIO7. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, Hi-Z
SPI1_MOSI/I2C1_SDA/GPIO8	C10	VDD_IO	I/O	I2C Control-Port Data. Data input/output for the I2C interface. SPI Control-Port Master Out Slave In. SPI data input. GPIO8. General-purpose input/output.	Programmable (pull-up, pull-down)	Output, Hi-Z
SPI1_SCK/GPIO9	C8	VDD_IO	I/O	SPI Control-Port Clock. Clock input for the SPI interface. GPIO9. General-purpose output.	Programmable (pull-up, pull-down)	Input, passive pull down
SPI1_SS/GPIO10	E6	VDD_IO	I/O	SPI Control-Port Slave Select. Active-low Slave Select input for the SPI interface. GPIO10. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, Hi-Z
SWIRE_CLK	D11	VDD_A ²	I	SoundWire Serial Clock. Clock input for the SoundWire peripheral interface. Optional clock reference for PLL.	—	Input, Hi-Z
SWIRE_DATA	F11	VDD_A	I/O	SoundWire Serial Data. Serial data input/output for the SoundWire peripheral interface.	—	Input, Hi-Z
SYNC/GPIO1	E4	VDD_IO	I/O	Multidevice Synchronization. Serial data bus connecting devices in multi-channel applications. GPIO1. General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
Analog I/O						
ADDR	E10	VDD_A	I	I2C Address Input/SoundWire ID Detect. Address pin for I2C Target address or SoundWire UNIQUE_ID instance number determination. Latched on POR or hard reset.	—	—
BST_SW	B1, B3	—	I	Boost Switch. Input to internal boost FETs.	—	—
LDO_D_FILT	F9	VDD_A	O	LDO_D Output. Decoupling point for digital supply, powered from LDO_D.	—	—
OUTN	D1	VBST	O	Differential Output. Internal Class D amplifier output.	—	—
OUTP	E2	VBST	O	Differential Output. Internal Class D amplifier output.	—	—

Table 1-1. CSP Ball Descriptions (Cont.)

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
VBST	C2, C4	—	O	Boosted Supply from Boost Converter. Internal boost converter output.	—	—
Power Supplies						
GND	F1, F3	—	—	Analog and Digital Ground. Ground return for the analog and digital functional blocks throughout the device.	—	—
GND_BST	A2, A4	—	—	Boost Converter Power Ground. Ground reference for the boost converter.	—	—
VDD_A	F7	—	I	Analog Supply. Power supply for the internal analog circuits. Also powers digital circuits via internal regulator.	—	—
VDD_P	F5	—	I	System Supply. Power supply for always-on (Hibernate) circuits.	—	—
VDD_B	A6	—	I	Boost Supply. Power supply for boost converter. (Note this is primarily a monitor pin; the boost current is conducted via the inductor to BST_SW.)	—	—
VDD_IO	B11	—	I	Digital I/O Supply. Power supply for digital input/output.	—	—

1. 5 V-tolerant input, supply-independent

2. SWIRE_CLK is powered from the VDD_A and VDD_IO supplies. Both supplies must be present before SWIRE_CLK is pulled high.

1.3 Alternative Pin Assignments for SoundWire-Only Applications

For SoundWire applications that do not require all the CS35L57 features, an alternative pin-assignment drawing is shown in Fig. 1-2. Unused balls towards the center of the chip package are grounded, allowing for simpler PCB design.

Note that the simplified pin assignment does not support functionality associated with the ASP, SPI control port, SYNC bus, interrupt output, or selected GPIO pins.

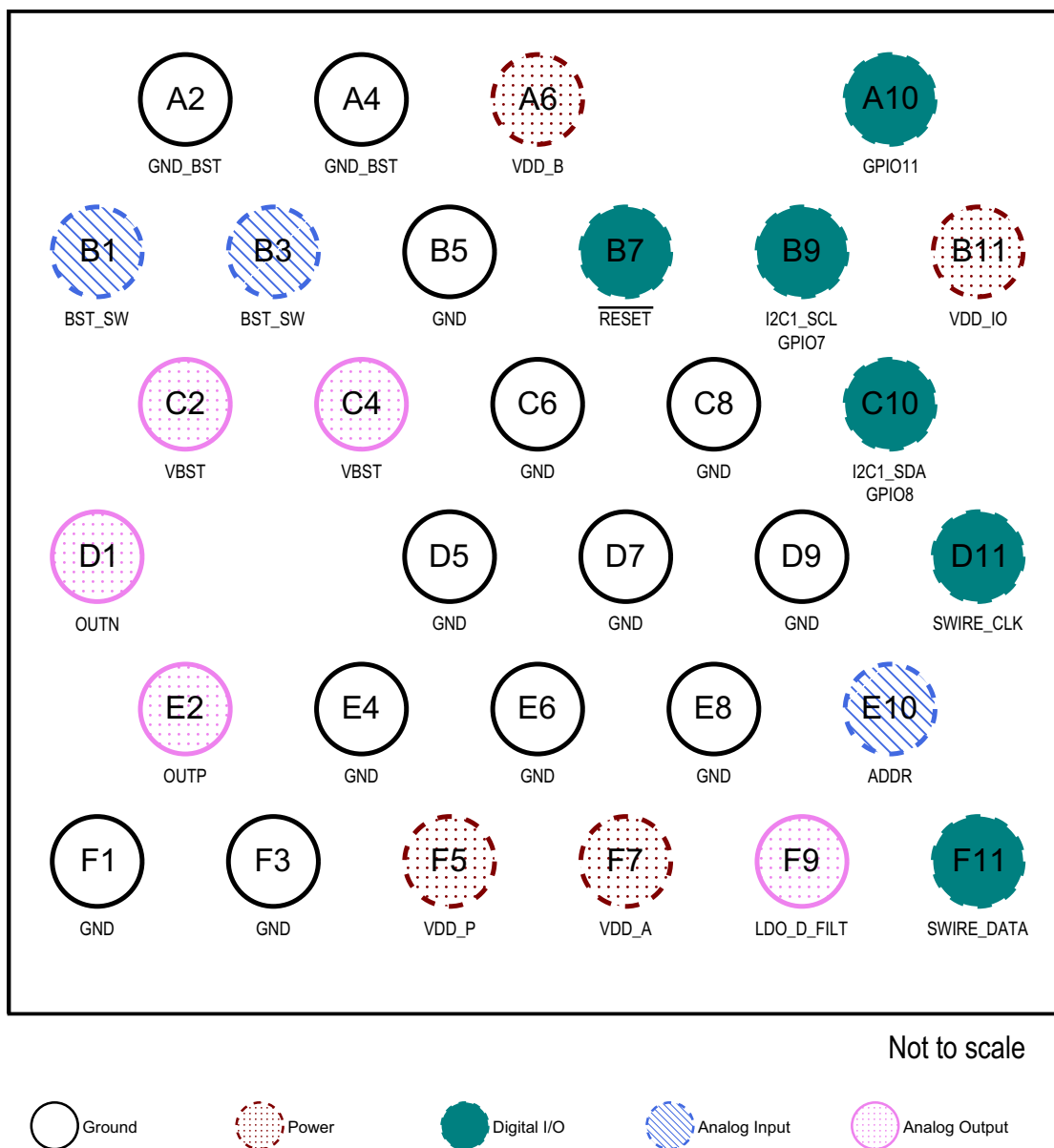


Figure 1-2. CSP 31-ball diagram (Top View, Through Package)

1.4 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
ASP1_BCLK/GPIO6 ASP1_DIN/GPIO3 ASP1_DOUT/GPIO4 ASP1_FSYNC/GPIO5	Float or connect to GND
ADDR SYNC/GPIO1 SPI1_MISO/I2C1_SCL/GPIO7 SPI1_SCK/GPIO9 GPIO11 GPIO12 SWIRE_CLK SWIRE_DATA	Connect to GND
SPI1_MOSI/I2C1_SDA/GPIO8	100 kΩ pull-down to GND
INT	100 kΩ pull-up to VDD_IO [1]
SPI1_SS/GPIO10	Connect to VDD_IO [2]

1. This pin can be connected to GND for SoundWire-only applications.

2. This pin can be connected to GND if unused, provided the SPI1_SCK/GPIO9 pin is also connected to GND.

1.5 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS35L57 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

2 Typical Connection Diagram

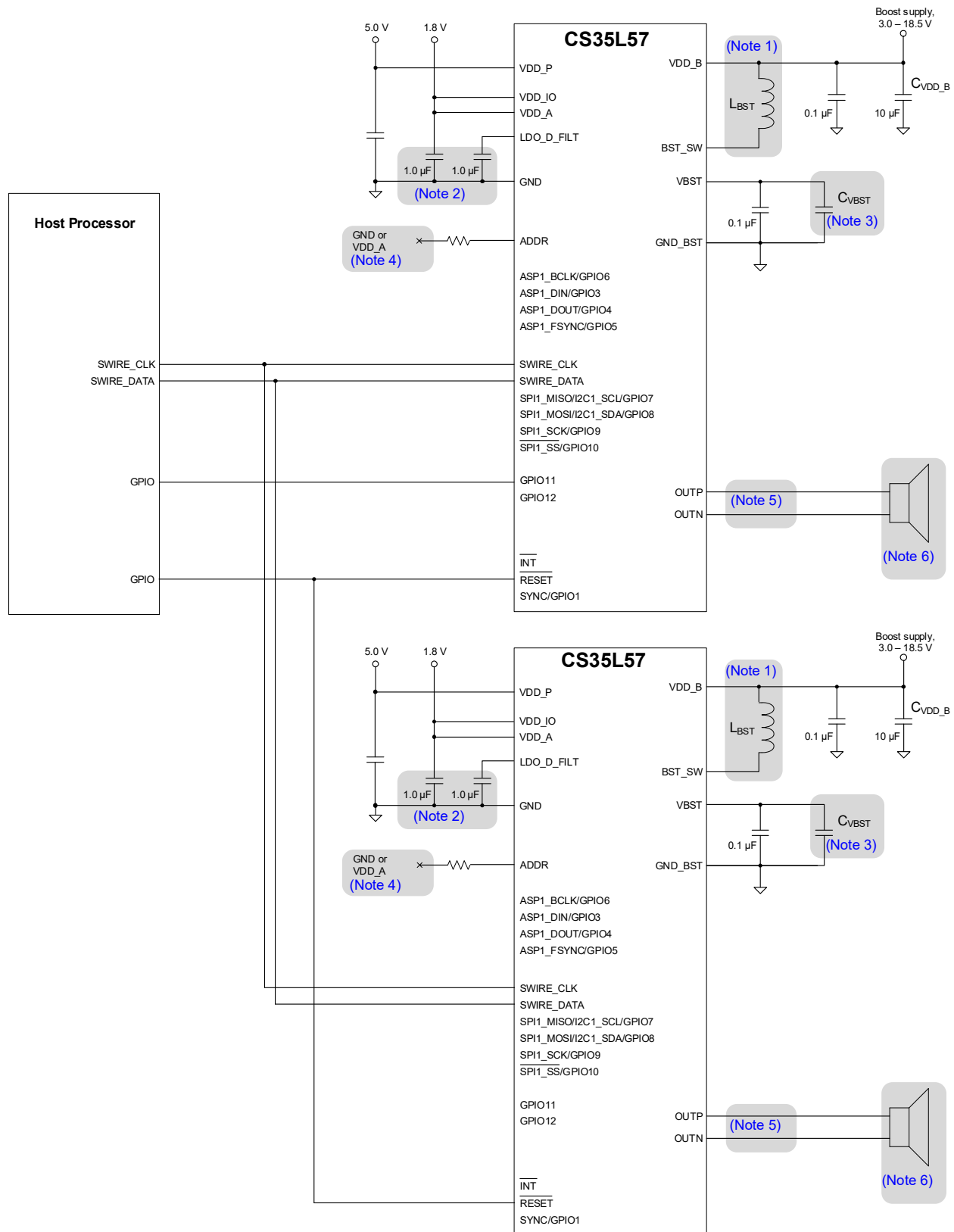


Figure 2-1. Stereo configuration with SoundWire control and internal boost power source

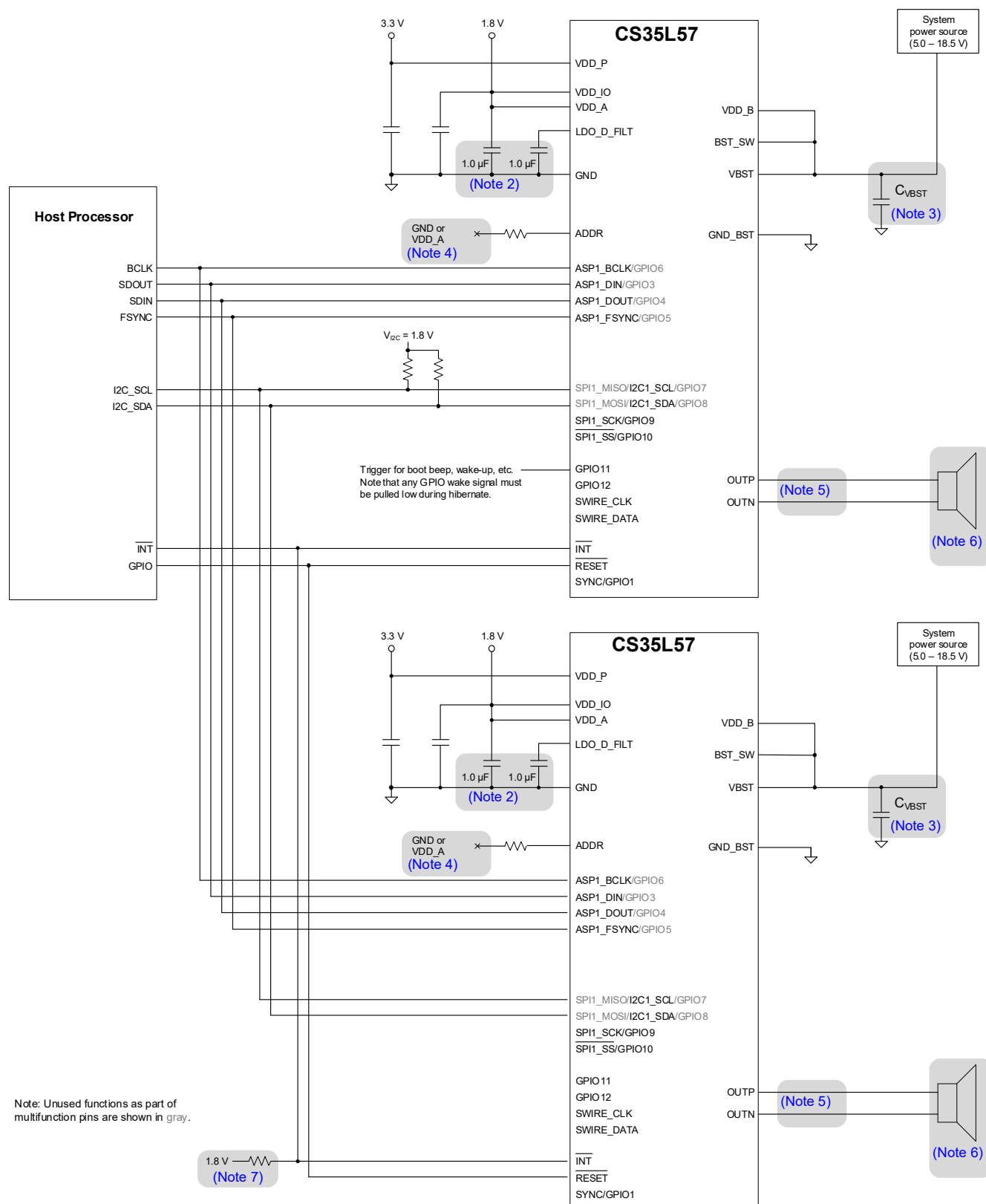


Figure 2-2. Stereo configuration with I²C control and external amplifier power source

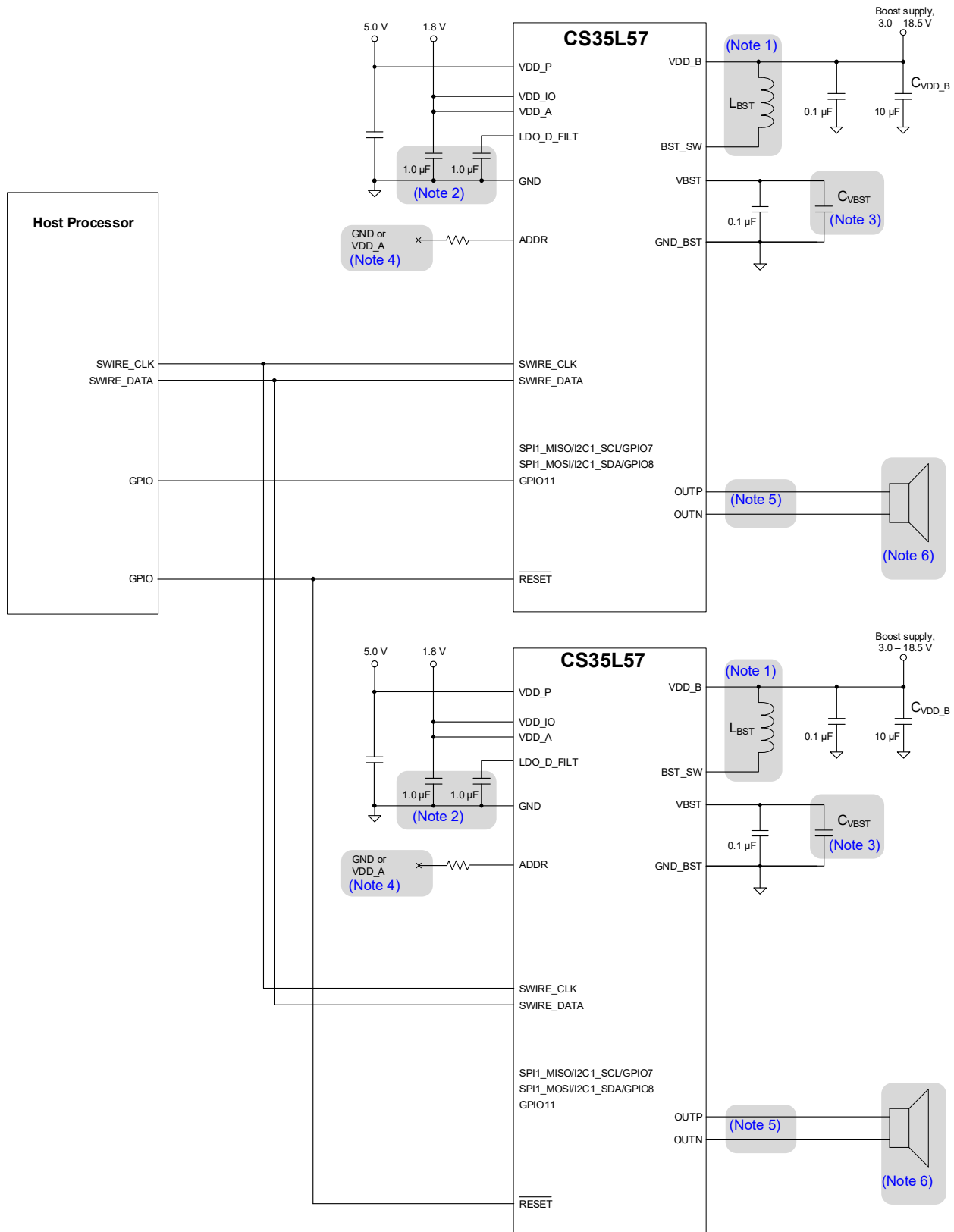


Figure 2-3. Stereo configuration with SoundWire control (reduced pin availability)

The typical connections shown in Fig. 2-3 are based on the pin assignments described in Section 1.3. The unsupported signal connections for this use case are not shown.

Notes referenced in the typical connection diagrams:

1. The L_{BST} inductor must not derate to a value less than 0.5 μ H. Inductance of 1.0 μ H is recommended for typical applications.
2. The VDD_A capacitor must not de-rate to a value less than 500 nF at 1.8 V. The LDO_D_FILT capacitor must not de-rate to a value less than 390 nF at 1.25 V.
3. The C_{VBST} capacitor must not derate to a value less than 2 μ F at 18.5 V.
4. The I²C device address and SoundWire unique instance ID are configured using a resistor connected between the ADDR pin and GND, or else between the ADDR pin and VDD_A. The capacitive loading on the ADDR pin must not exceed 100 pF.
5. Optional EMI-suppression capacitors between OUTx and GND may be used, depending on the application requirements. The capacitance should not exceed 470 pF, as higher capacitance increases switching losses.
6. When using a simulated load of 8 Ω + 33 μ H, a Coilcraft DO5040H–333MLB inductor is used.
7. In the configuration shown, the CS35L57 $\overline{INT}$ pin is configured as an open-drain output and an external pull-up resistor (e.g., 100 k Ω) to VDD_IO is required.

General notes and recommendations:

- Fig. 2-1 through Fig. 2-3 are examples intended to describe the connectivity of each functional block within the CS35L57, and do not limit all possible use cases.
- All external passive component values listed are nominal values.

3 Characteristics and Specifications

Note: The default register field configurations are used unless specified otherwise in the test conditions.

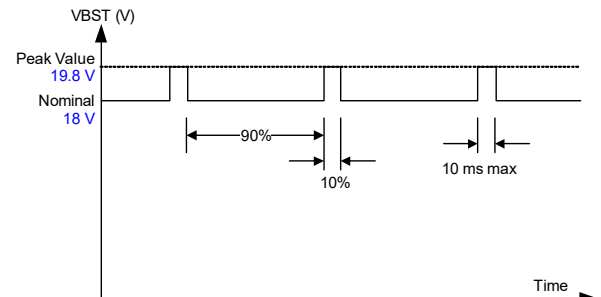
Table 3-1. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_BST = 0 V; voltages are with respect to ground.

Parameter ¹		Symbol	Minimum	Maximum	Unit
DC power supply	Analog and digital supply	VDD_P	3.0	5.5	V
	Digital I/O supply	VDD_IO	1.71	3.6	V
	Analog supply	VDD_A	1.71	1.89	V
	Boost converter ^{2,3}	VDD_B	3.0	18.5	V
	Amplifier supply ^{3,4,5}	VBST	5.0	18.5	V
Supply ramp up/down		VDD_P, VDD_IO, VDD_A VDD_B, VBST	t _{PWR-UD}	0.1 0.2	100 100
External voltage applied to digital input/output	VDD_IO input/output pins ⁶	V _{INDI}	-0.3	VDD_IO + 0.3	V
	RESET pin		-0.3	5.5	V
	VDD_A input/output pins ⁷		-0.3	VDD_A + 0.3	V
External voltage applied to analog inputs	ADDR pin	V _{INAI}	-0.3	VDD_A + 0.3	V
External voltage applied to analog outputs	OUTP, OUTN pins	V _{IN-OUTx}	-0.3	VBST + 0.3	V
Ambient temperature		T _A	-40	+85	°C

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

- There are no sequencing requirements associated with any of the supplies—each can be enabled or removed independently of the other supplies.
- Note VDD_B is the voltage-monitor point for the boost converter; the load current path is through the inductor to the BST_SW.
- The amplifier supply can be generated by the boost converter, or else provided externally. When using an external amplifier supply, the VDD_B, BST_SW, and VBST pins must be connected together.
- Note the VBST voltage may exceed these operating limits if generated by the CS35L57 boost converter.
- If VBST is provided externally at 18.0 V (nominal), the CS35L57 can withstand voltage spikes of 19.8 V with duration 10 ms (maximum) and 10% duty cycle.



- All digital I/O pins except RESET, SWIRE_DAT and SWIRE_CLK.
- SWIRE_CLK, SWIRE_DATA

4 Package Dimensions

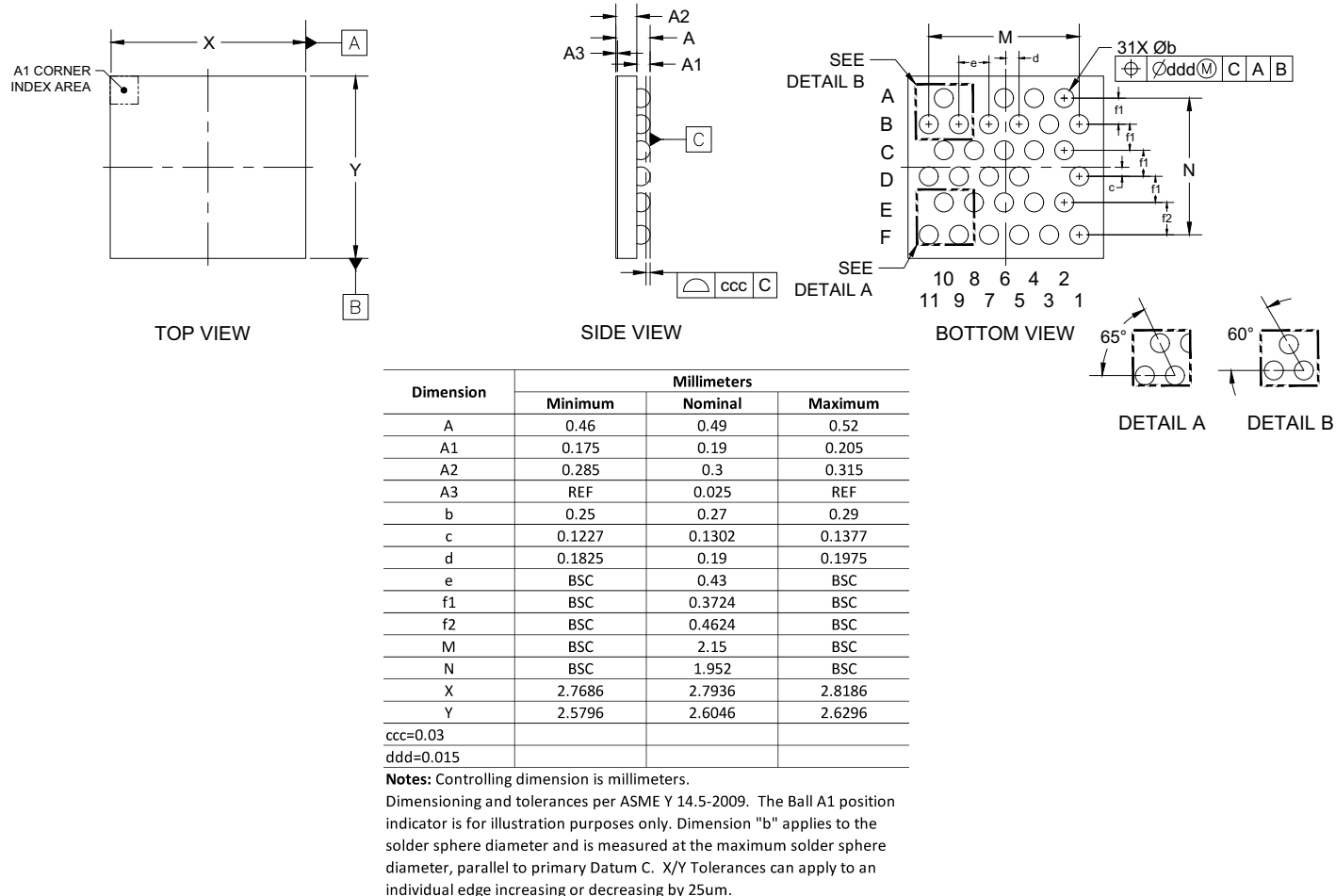


Figure 4-1. CSP Package Drawing

5 Ordering Information

Table 5-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS35L57	18.5 V Class D Smart Amplifier with Multi-Cell Battery Boost	31-ball CSP	Yes	Commercial	-40 to +85°C	Tape and Reel	CS35L57-CWR

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

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