CS5340

101 dB, 192 kHz, Multi-Bit Audio A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-bit Conversion
- Supports All Audio Sample Rates Including 192 kHz
- 101 dB Dynamic Range at 5 V
- -94 dB THD+N
- 90 mW Power Consumption
- High-Pass Filter to Remove DC Offsets
- Analog/Digital Core Supplies from 3.3 V to 5 V
- Supports Logic Levels between 1.8 V and 5 V
- Auto-detect Mode Selection in Slave Mode
- Auto-Detect MCLK Divider
- Pin Compatible with CS5341

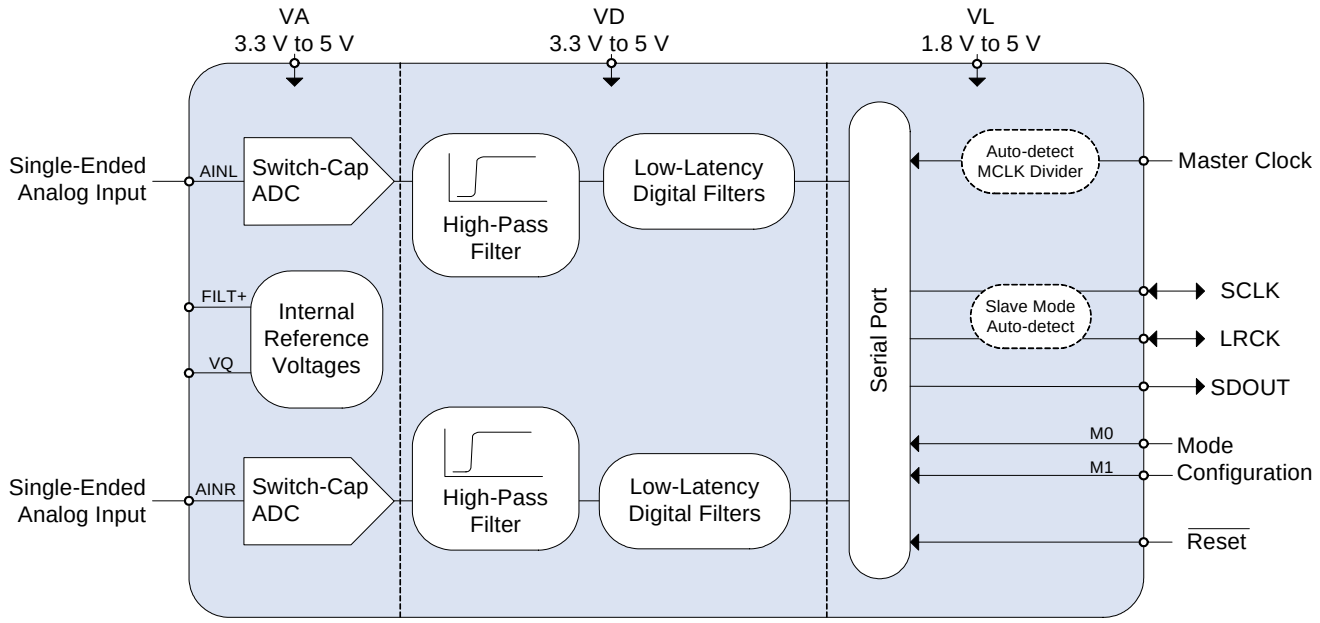
General Description

The CS5340 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 200 kHz per channel.

The CS5340 uses a 5th-order, multi-bit Delta-Sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5340 is available in a 16-pin TSSOP package for Commercial (-10° to +70° C) and Automotive grades (-40° to +85° C). The CDB5340 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 22 for complete ordering information.

The CS5340 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as set-top boxes, DVD-karaoke players, DVD recorders, A/V receivers, and automotive applications.



Copyright © Cirrus Logic, Inc. 2008
(All Rights Reserved)

TABLE OF CONTENTS

1. CHARACTERISTICS AND SPECIFICATIONS 4
SPECIFIED OPERATING CONDITIONS 4
ABSOLUTE MAXIMUM RATINGS 4
ANALOG CHARACTERISTICS - COMMERCIAL GRADE 5
ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE 6
DIGITAL FILTER CHARACTERISTICS 7
DC ELECTRICAL CHARACTERISTICS 10
DIGITAL CHARACTERISTICS 10
SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT 11
2. PIN DESCRIPTION 13
3. TYPICAL CONNECTION DIAGRAM 14
4. APPLICATIONS 15
4.1 Single-, Double-, and Quad-Speed Modes 15
4.2 Operation as Either a Clock Master or Slave 15
4.2.1 Operation as a Clock Master 16
4.2.2 Operation as a Clock Slave with Auto-Detect 16
4.2.3 Master Clock 17
4.3 Serial Audio Interface 17
4.4 Power-Up Sequence 18
4.5 Analog Connections 18
4.6 Grounding and Power Supply Decoupling 18
4.7 Synchronization of Multiple Devices 18
4.8 Capacitor Size on the Reference Pin (FILT+) 19
5. PARAMETER DEFINITIONS 20
6. PACKAGE DIMENSIONS 21
THERMAL CHARACTERISTICS 21
7. ORDERING INFORMATION 22
8. REVISION HISTORY 22

LIST OF FIGURES

Figure 1.Single-Speed Mode Stopband Rejection 8
Figure 2.Single-Speed Mode Stopband Rejection 8
Figure 3.Single-Speed Mode Transition Band (Detail) 8
Figure 4.Single-Speed Mode Passband Ripple 8
Figure 5.Double-Speed Mode Stopband Rejection 8
Figure 6.Double-Speed Mode Stopband Rejection 8
Figure 7.Double-Speed Mode Transition Band (Detail) 9
Figure 8.Double-Speed Mode Passband Ripple 9
Figure 9.Quad-Speed Mode Stopband Rejection 9
Figure 10.Quad-Speed Mode Stopband Rejection 9
Figure 11.Quad-Speed Mode Transition Band (Detail) 9
Figure 12.Quad-Speed Mode Passband Ripple 9
Figure 13.Master Mode, Left-Justified SAI 12
Figure 14.Slave Mode, Left-Justified SAI 12
Figure 15.Master Mode, I²S SAI 12
Figure 16.Slave Mode, I²S SAI 12
Figure 17.Typical Connection Diagram 14
Figure 18.CS5340 Master Mode Clocking 16
Figure 19.I²S Serial Audio Interface 17
Figure 20.Left-Justified Serial Audio Interface 17
Figure 21.CS5340 Recommended Analog Input Buffer 18
Figure 22.CS5340 THD+N versus Frequency 19

LIST OF TABLES

Table 1. Speed Modes and the Associated Output Sample Rates (Fs) 15
Table 2. CS5340 Mode Control 15
Table 3. Master Clock (MCLK) Ratios 17
Table 4. Master Clock (MCLK) Frequencies for Standard Audio Sample Rates 17

1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Analog	VA	3.1	(Note 1)	5.25	V
	Digital	VD	3.1	3.3	5.25	V
	Logic	VL	1.7	3.3	5.25	V
Ambient Operating Temperature	Commercial	T_{AC}	-10	-	70	°C
	Automotive	T_{AC}	-40	-	85	°C

Notes:

1. This part is specified at typical analog voltages of 3.3 V and 5.0 V. See *Analog Characteristics - Commercial Grade* and *Analog Characteristics - Automotive Grade,* below, for details.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V, All voltages with respect to ground.) (Note 2)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Logic	VL	-0.3	+6.0	V
	Digital	VD	-0.3	+6.0	V
Input Current	(Note 3)	I_{in}	-10	+10	mA
Analog Input Voltage	(Note 4)	V_{IN}	GND-0.7	VA+0.7	V
Digital Input Voltage	(Note 4)	V_{IND}	-0.7	VL+0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

2. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.
4. The maximum over/under voltage is limited by the input current.

ANALOG CHARACTERISTICS - COMMERCIAL GRADE

Test Conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

Dynamic Performance for Commercial Grade			VA = 5 V			VA = 3.3 V			
Single-Speed Mode	***Fs = 48 kHz***	***Symbol***	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Dynamic Range	A-weighted		95	101	-	92	98	-	dB
	unweighted		92	98	-	89	95	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N							
	-1 dB		-	-94	-88	-	-91	-85	dB
	-20 dB		-	-78	-	-	-75	-	dB
	-60 dB		-	-38	-	-	-35	-	dB
Double-Speed Mode	***Fs = 96 kHz***	***Symbol***	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Dynamic Range	A-weighted		95	101	-	92	98	-	dB
	unweighted		92	98	-	89	95	-	dB
	40 kHz bandwidth unweighted		-	95	-	-	92	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N							
	-1 dB		-	-94	-88	-	-91	-85	dB
	-20 dB		-	-78	-	-	-75	-	dB
	-60 dB		-	-38	-	-	-35	-	dB
	40 kHz bandwidth -1 dB		-	-91	-	-	-85	-	dB
Quad-Speed Mode	***Fs = 192 kHz***	***Symbol***	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Dynamic Range	A-weighted		95	101	-	92	98	-	dB
	unweighted		92	98	-	89	95	-	dB
	40 kHz bandwidth unweighted		-	95	-	-	92	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N							
	-1 dB		-	-94	-88	-	-91	-85	dB
	-20 dB		-	-78	-	-	-75	-	dB
	-60 dB		-	-38	-	-	-35	-	dB
	40 kHz bandwidth -1 dB		-	-91	-	-	-85	-	dB

Dynamic Performance All Modes	***Min***	***Typ***	***Max***	***Unit***
Interchannel Isolation	-	90	-	dB
DC Accuracy				
Interchannel Gain Mismatch	-	0.1	-	dB
Gain Error	-5	-	+5	%
Gain Drift	-	±100	-	ppm/°C
Analog Input Characteristics				
Full-Scale Input Voltage	0.53*VA	0.56*VA	0.59*VA	Vpp
Input Impedance	-	25	-	kΩ

5. Referred to the typical full-scale input voltage

ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE

Test Conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

Dynamic Performance for Automotive Grade			VA = 5 V			VA = 3.3 V			
Single-Speed Mode	***Fs = 48 kHz***	***Symbol***	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Dynamic Range	A-weighted		93	101	-	90	98	-	dB
	unweighted		90	98	-	87	95	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N							
	-1 dB		-	-94	-86	-	-91	-83	dB
	-20 dB		-	-78	-	-	-75	-	dB
	-60 dB		-	-38	-	-	-35	-	dB
Double-Speed Mode	***Fs = 96 kHz***	***Symbol***	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Dynamic Range	A-weighted		93	101	-	90	98	-	dB
	unweighted		90	98	-	87	95	-	dB
	40 kHz bandwidth unweighted		-	95	-	-	92	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N							
	-1 dB		-	-94	-86	-	-91	-83	dB
	-20 dB		-	-78	-	-	-75	-	dB
	-60 dB		-	-38	-	-	-35	-	dB
	40 kHz bandwidth -1 dB		-	-91	-	-	-85	-	dB
Quad-Speed Mode	***Fs = 192 kHz***	***Symbol***	***Min***	***Typ***	***Max***	***Min***	***Typ***	***Max***	***Unit***
Dynamic Range	A-weighted		93	101	-	90	98	-	dB
	unweighted		90	98	-	87	95	-	dB
	40 kHz bandwidth unweighted		-	95	-	-	92	-	dB
Total Harmonic Distortion + Noise	(Note 5)	THD+N							
	-1 dB		-	-94	-86	-	-91	-83	dB
	-20 dB		-	-78	-	-	-75	-	dB
	-60 dB		-	-38	-	-	-35	-	dB
	40 kHz bandwidth -1 dB		-	-91	-	-	-85	-	dB

Dynamic Performance All Modes	***Min***	***Typ***	***Max***	***Unit***
Interchannel Isolation	-	90	-	dB
DC Accuracy				
Interchannel Gain Mismatch	-	0.1	-	dB
Gain Error	-10	-	+10	%
Gain Drift	-	±100	-	ppm/°C
Analog Input Characteristics				
Full-Scale Input Voltage	0.50*VA	0.56*VA	0.62*VA	Vpp
Input Impedance	-	25	-	kΩ

6. Referred to the typical full-scale input voltage

DIGITAL FILTER CHARACTERISTICS

Parameter			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)	(Note 7)		0	-	0.4895	Fs
Passband Ripple				-0.035	-	0.035	dB
Stopband		(Note 7)		0.5687	-	-	Fs
Stopband Attenuation				70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)	(Note 7)		0	-	0.4895	Fs
Passband Ripple				-0.025	-	0.025	dB
Stopband		(Note 7)		0.5604	-	-	Fs
Stopband Attenuation				69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	9/Fs	-	s
Quad-Speed Mode							
Passband	(-0.1 dB)	(Note 7)		0	-	0.2604	Fs
Passband Ripple				-0.025	-	0.025	dB
Stopband		(Note 7)		0.5	-	-	Fs
Stopband Attenuation				60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB -0.13 dB	(Note 8)		-	1 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 8)		-	10	-	Deg
Passband Ripple				-	-	0	dB

7. Filter characteristics scale precisely with Fs
8. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

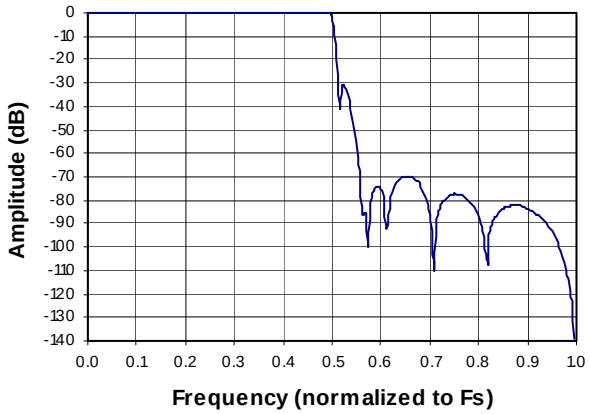


Figure 1. Single-Speed Mode Stopband Rejection

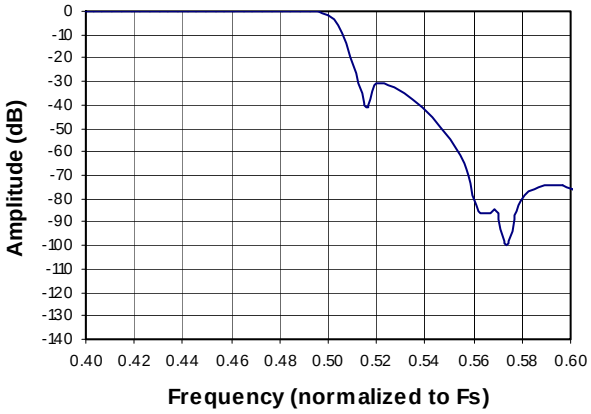


Figure 2. Single-Speed Mode Stopband Rejection

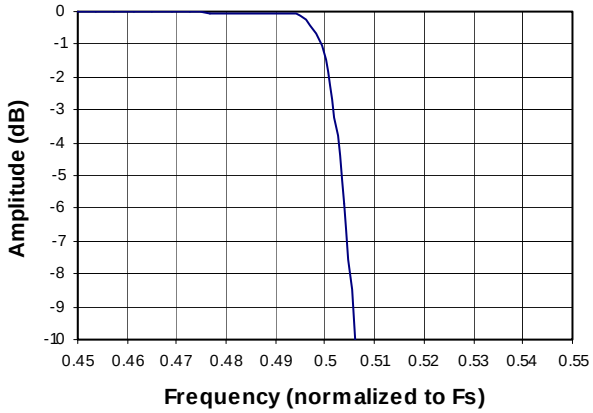


Figure 3. Single-Speed Mode Transition Band (Detail)

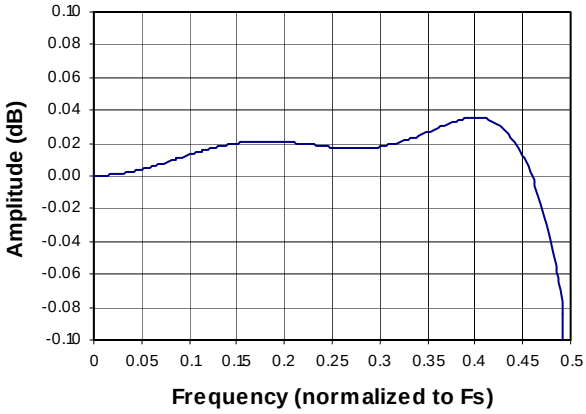


Figure 4. Single-Speed Mode Passband Ripple

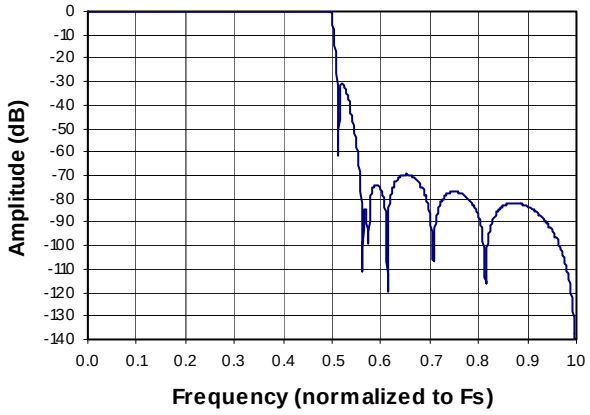


Figure 5. Double-Speed Mode Stopband Rejection

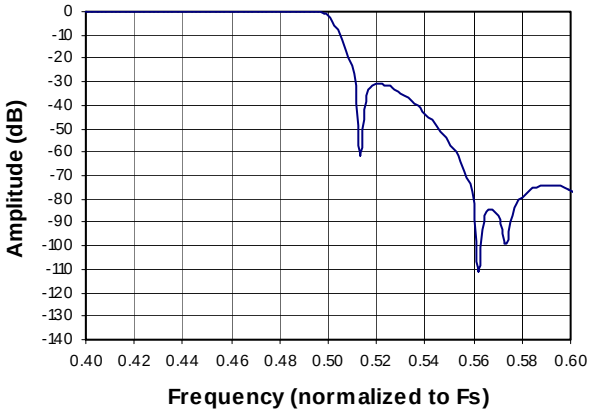


Figure 6. Double-Speed Mode Stopband Rejection

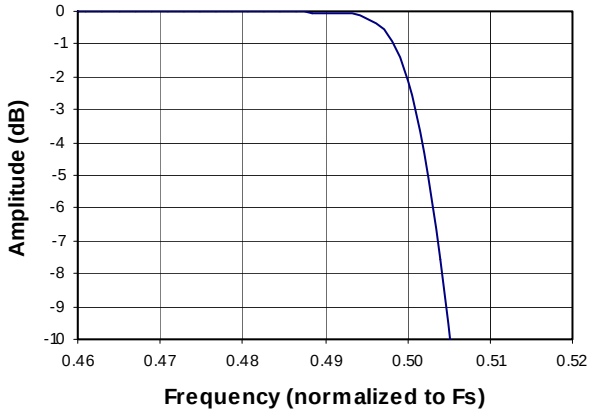


Figure 7. Double-Speed Mode Transition Band (Detail)

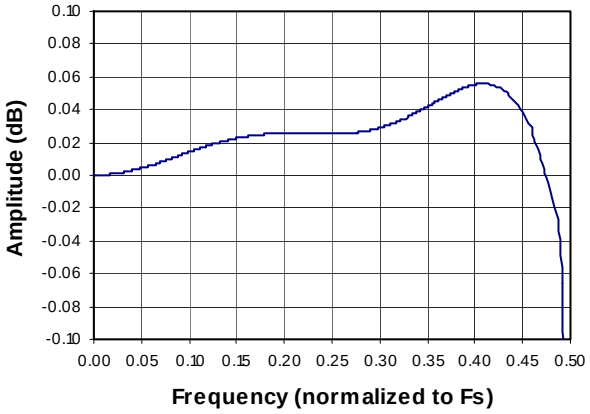


Figure 8. Double-Speed Mode Passband Ripple

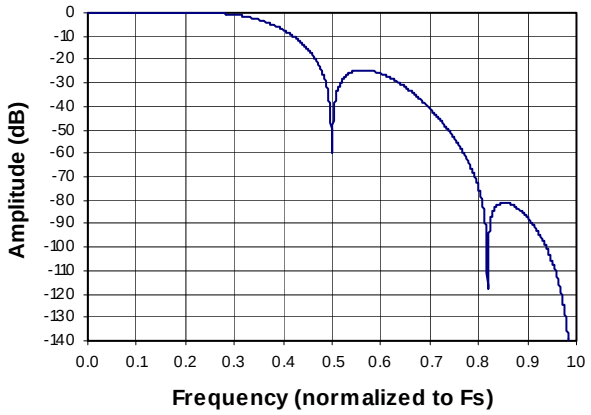


Figure 9. Quad-Speed Mode Stopband Rejection

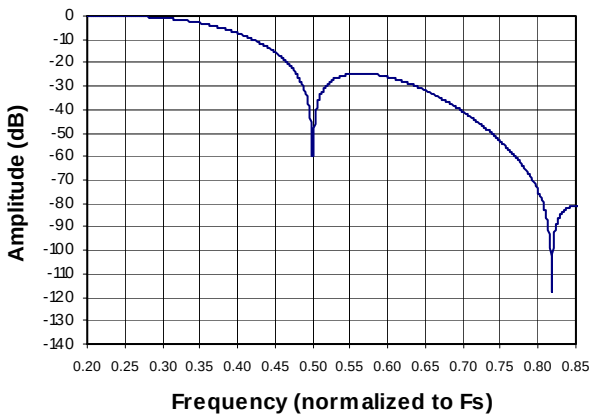


Figure 10. Quad-Speed Mode Stopband Rejection

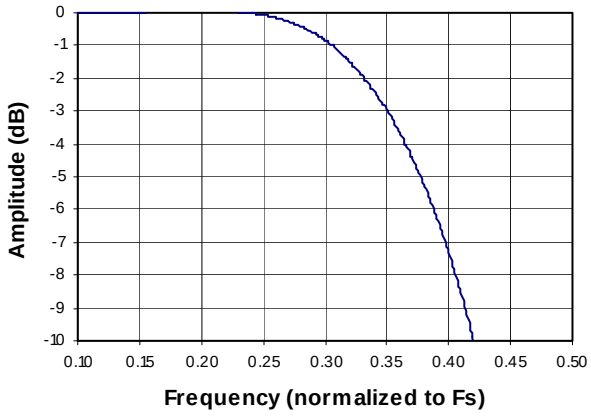


Figure 11. Quad-Speed Mode Transition Band (Detail)

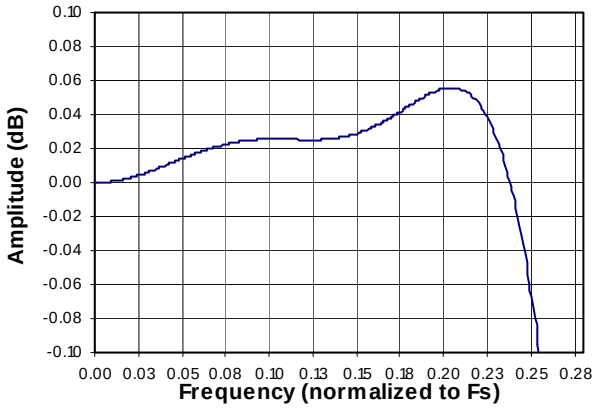


Figure 12. Quad-Speed Mode Passband Ripple

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to 0 V. MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	3.1	-	5.25	V
	Positive Digital	VD	3.1	-	5.25	V
	Positive Logic	VL	1.7	-	5.25	V
Power Supply Current	VA = 5 V	I_A	-	21	25.5	mA
(Normal Operation)	VA = 3.3 V	I_A	-	18.2	22.5	mA
	VL,VD = 5 V	I_D	-	15	18.5	mA
	VL,VD = 3.3 V	I_D	-	9	10	mA
Power Supply Current	VA = 5 V	I_A	-	1.5	-	mA
(Power-Down Mode) (Note 9)	VL,VD=5 V	I_D	-	0.4	-	mA
Power Consumption	VL, VD, VA = 5 V	-	-	180	220	mW
(Normal Operation)	VL, VD, VA = 3.3 V	-	-	90	107.2	mW
	(Power-Down Mode)	-	-	9.5	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 10)	PSRR	-	65	-	dB
V_Q Nominal Voltage			-	VA÷2	-	V
Output Impedance			-	25	-	kΩ
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	36	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

9. Power Down Mode is defined as $\overline{RST}$ = Low, with all clocks and data lines held static at a valid logic levels.
10. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram, Figure 17 on page 14.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 100 µA	(% of VL)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_o =100 µA	(% of VL)	V_{OL}	-	-	15%	V
Input Leakage Current		I_{in}	-10	-	+10	µA

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(Logic "0" = GND = 0 V; Logic "1" = VL, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
MCLK Specifications						
MCLK Period		t_{clkw}	39	-	45	ns
			78	-	1953	ns
MCLK Pulse Duty Cycle			40	-	60	%
Master Mode						
SCLK falling to LRCK	Single-Speed	t_{mslr}	-20	-	20	ns
	Double-Speed		-20	-	20	ns
	Quad-Speed		-8	-	8	ns
SCLK falling to SDOUT valid.		t_{sdo}	-	-	32	ns
SCLK Duty Cycle.	Single-Speed		-	50	-	%
	Double-Speed		-	50	-	%
	Quad-Speed		-	33	-	%
Slave Mode						
Single-Speed (Note 11)						
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclkw}	156	-	-	ns
SCLK Duty Cycle			45	50	55	%
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SCLK falling to LRCK edge		t_{slrd}	-20	-	20	ns
Double-Speed (Note 11)						
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclkw}	156	-	-	ns
SCLK Duty Cycle			45	50	55	%
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SCLK falling to LRCK edge.		t_{slrd}	-20	-	20	ns
Quad-Speed (Note 11)						
LRCK Duty Cycle			40	50	60	%
SCLK Period		t_{sclkw}	78	-	-	ns
SCLK Duty Cycle			29.7	33	50	%
SDOUT valid before SCLK rising		t_{stp}	10	-	-	ns
SDOUT valid after SCLK rising		t_{hld}	5	-	-	ns
SCLK falling to LRCK edge.		t_{slrd}	-8	-	8	ns

11. For a description of speed modes, please refer to Table on page 15.

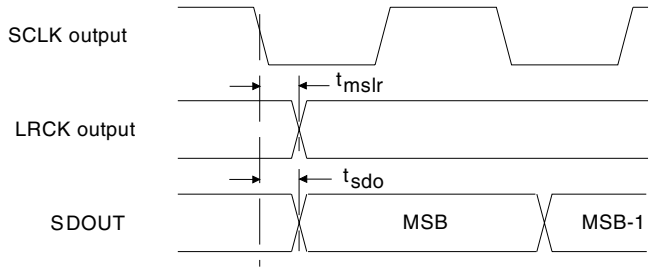


Figure 13. Master Mode, Left-Justified SAI

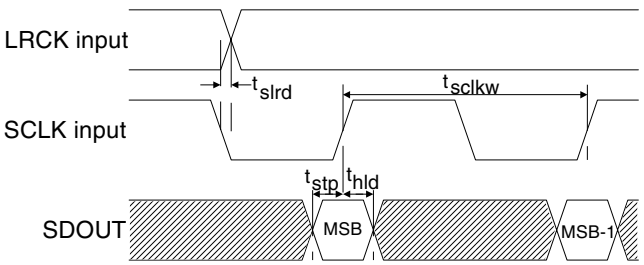


Figure 14. Slave Mode, Left-Justified SAI

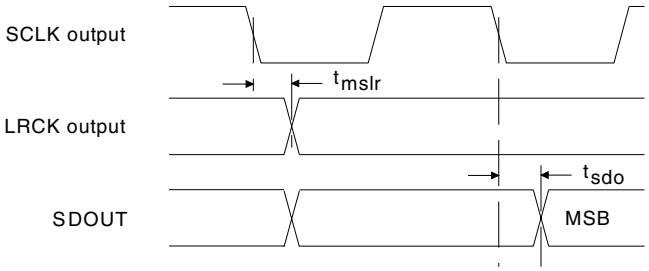


Figure 15. Master Mode, I²S SAI

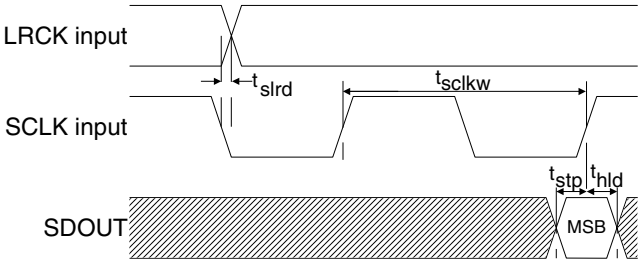
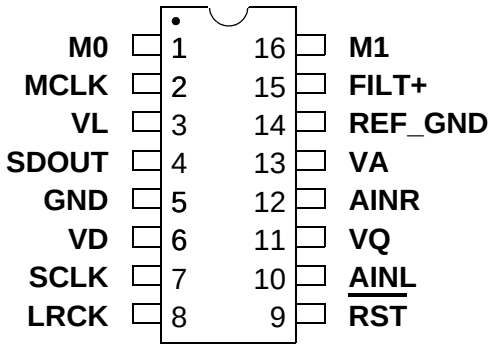


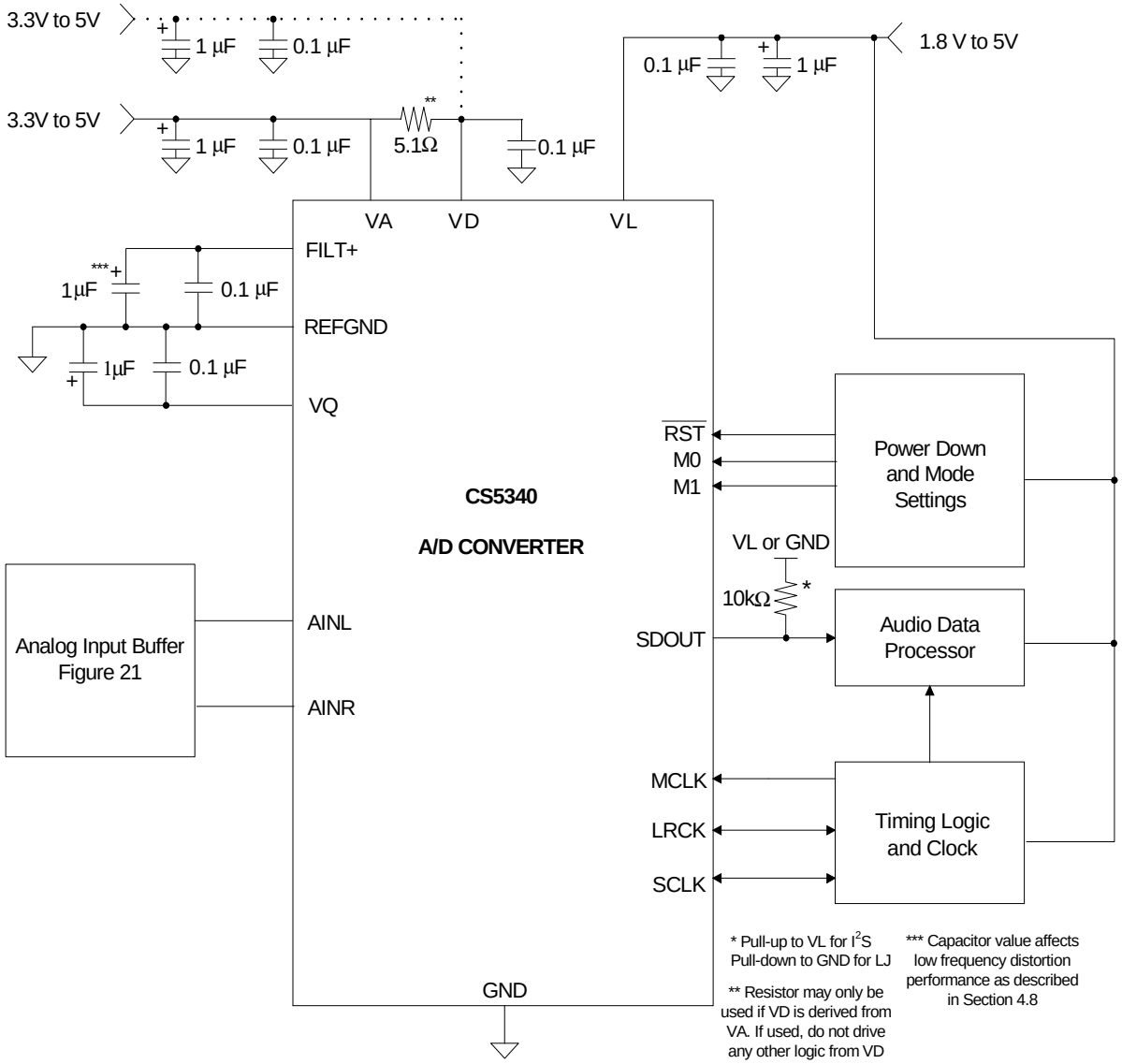
Figure 16. Slave Mode, I²S SAI

2. PIN DESCRIPTION



Pin Name	#	Pin Description
M0 M1	1 16	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MCLK	2	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VL	3	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	4	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
GND	5,14	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
SCLK	7	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
LRCK	8	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
$\overline{\text{RST}}$	9	**Reset** (*Input*) - The device enters a low power mode when low.
AINL AINR	10 12	**Analog Input** (*Input*) - The full-scale analog input level is specified in the Analog Characteristics specification table.
VQ	11	**Quiescent Voltage** *(Output)* **-** Filter connection for the internal quiescent reference voltage.
VA	13	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
FILT+	15	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

3. TYPICAL CONNECTION DIAGRAM



4. APPLICATIONS

4.1 Single-, Double-, and Quad-Speed Modes

The CS5340 can support output sample rates from 2 kHz to 200 kHz. The proper speed mode can be determined by the desired output sample rate and the external MCLK/LRCK ratio, as shown in Table 1.

Speed Mode	MCLK/LRCK Ratio	Output Sample Rate Range (kHz)
Single-Speed Mode	512x	43 - 50
	256x	2 - 50
Double-Speed Mode	256x	86 - 100
	128x	4 - 100
Quad-Speed Mode	128x	172 - 200
	64x*	100 - 200
* Quad-Speed Mode, 64x only available in Master Mode.		

Table 1. Speed Modes and the Associated Output Sample Rates (Fs)

4.2 Operation as Either a Clock Master or Slave

The CS5340 supports operation as either a clock master or slave. As a clock master, the LRCK and SCLK pins are outputs with the left/right and serial clocks synchronously generated on-chip. As a clock slave, the LRCK and SCLK pins are inputs and require the left/right and serial clocks to be externally generated. The selection of clock master or slave is made via the Mode pins as shown in Table 2.

M1 (Pin 16)	M0 (Pin 1)	MODE
0	0	Clock Master, Single-Speed Mode
0	1	Clock Master, Double-Speed Mode
1	0	Clock Master, Quad-Speed Mode
1	1	Clock Slave, All Speed Modes

Table 2. CS5340 Mode Control

4.2.1 Operation as a Clock Master

As a clock master, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 18.

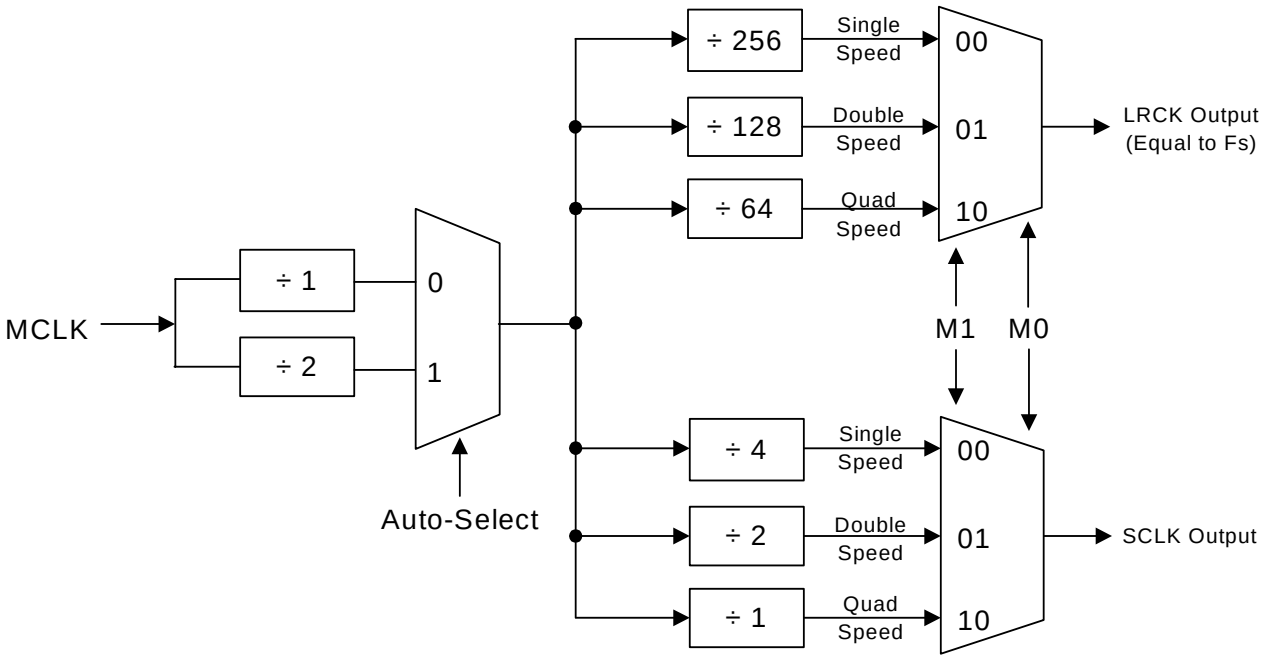


Figure 18. CS5340 Master Mode Clocking

4.2.2 Operation as a Clock Slave with Auto-Detect

LRCK and SCLK operate as inputs in clock slave mode. It is recommended that the left/right clock be synchronously derived from the master clock and must be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance.

A unique feature of the CS5340 is the automatic selection of either Single-, Double- or Quad-Speed mode when operating as a clock slave. The auto-mode select feature negates the need to configure the Mode pins to correspond to the desired mode. The auto-mode selection feature supports all standard audio sample rates from 2 to 200 kHz. However, there are ranges of non-standard audio sample rates that are not supported when operating with a fast MCLK (512x, 256x, 128x for Single-, Double-, and Quad-Speed Modes, respectively). Please refer to Table for supported sample rate ranges.

4.2.3 Master Clock

The CS5340 requires a Master clock (MCLK) which runs the internal sampling circuits and digital filters. There is also an internal MCLK divider which is automatically activated based on the speed mode and frequency of the MCLK. Table 3 shows a listing of the external MCLK/LRCK ratios that are required. Table 4 lists some common audio output sample rates and the required MCLK frequency. Please note that not all of the listed sample rates are supported when operating with a fast MCLK (512x, 256x, 128x for Single-, Double-, and Quad-Speed Modes, respectively).

	Single-Speed Mode	Double-Speed Mode	Quad-Speed Mode
MCLK/LRCK Ratio	256x, 512x	128x, 256x	64x*,128x
* Quad Speed, 64x only available in Master Mode.			

Table 3. Master Clock (MCLK) Ratios

SAMPLE RATE (kHz)	MCLK (MHz)
32	8.192
44.1	11.2896 22.5792
48	12.288 24.576
64	8.192
88.2	11.2896 22.5792
96	12.288 24.576
192	12.288 24.576

Table 4. Master Clock (MCLK) Frequencies for Standard Audio Sample Rates

4.3 Serial Audio Interface

The CS5340 supports both I²S and Left-Justified serial audio formats. Upon start-up, the CS5340 will detect the logic level on SDOUT (pin 4). A 10 kΩ pull-up to VL is needed to select I²S format, and a 10 kΩ pull-down to GND is needed to select Left-Justified format. Figures 19 and 20 illustrate the I²S and Left-Justified audio formats. Please see Figures 13 through 16, for more information on the required timing for the two serial audio interface formats. Also see Application Note AN282 for a detailed discussion of the serial audio interface formats.

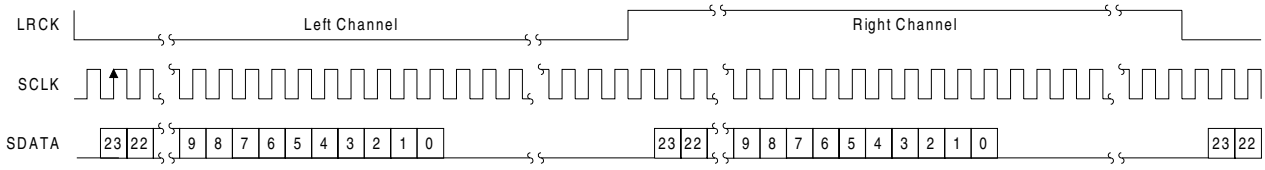


Figure 19. I²S Serial Audio Interface

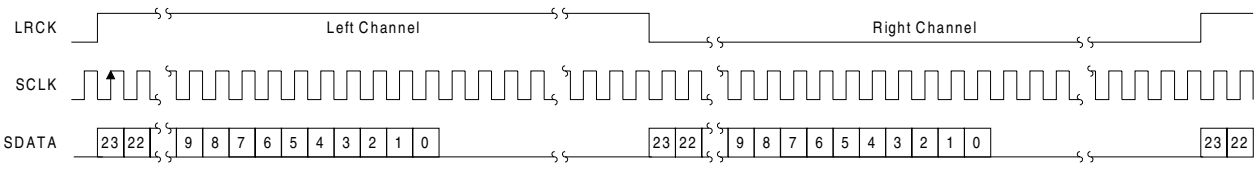


Figure 20. Left-Justified Serial Audio Interface

4.4 Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power-glitch-related issues.

4.5 Analog Connections

The analog modulator samples the input at half of the MCLK frequency, or nominally 6.144 MHz. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the input sampling frequency (n × 6.144 MHz), where n=0,1,2,... Refer to Figure 21 which shows the suggested filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

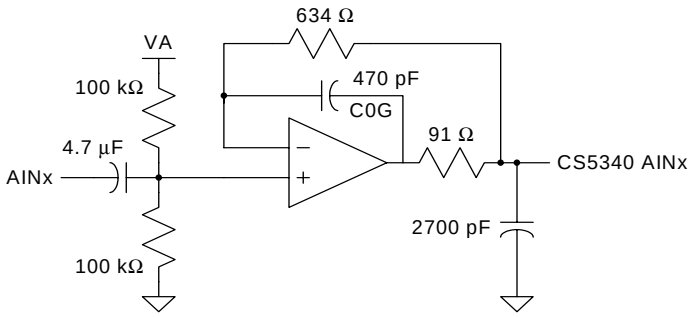


Figure 21. CS5340 Recommended Analog Input Buffer

4.6 Grounding and Power Supply Decoupling

As with any high-resolution converter, achieving optimal performance from the CS5340 requires careful attention to power supply and grounding arrangements. Figure 17 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low-value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from FILT+ and REF_GND. Furthermore, all ground pins on CS5340 should be referenced to the same ground reference. The CDB5340 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

4.7 Synchronization of Multiple Devices

In systems where multiple ADCs are required, the user can achieve simultaneous sampling if the MCLK and LRCK signals are the same for all of the CS5340's in the system. If only one master clock source is needed, one solution is to place one CS5340 in Master mode, and slave all of the other CS5340's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5340 reset with the inactive (falling) edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

4.8 Capacitor Size on the Reference Pin (FILT+)

The CS5340 requires an external capacitance on the internal reference voltage pin, FILT+. The size of this decoupling capacitor will affect the low frequency distortion performance as shown in Figure 22, with larger capacitor values used to optimize low frequency distortion performance. This plot was taken using the CDB5340 evaluation platform, with the device running in Single-Speed Mode and VA=VD=VL=5 V.

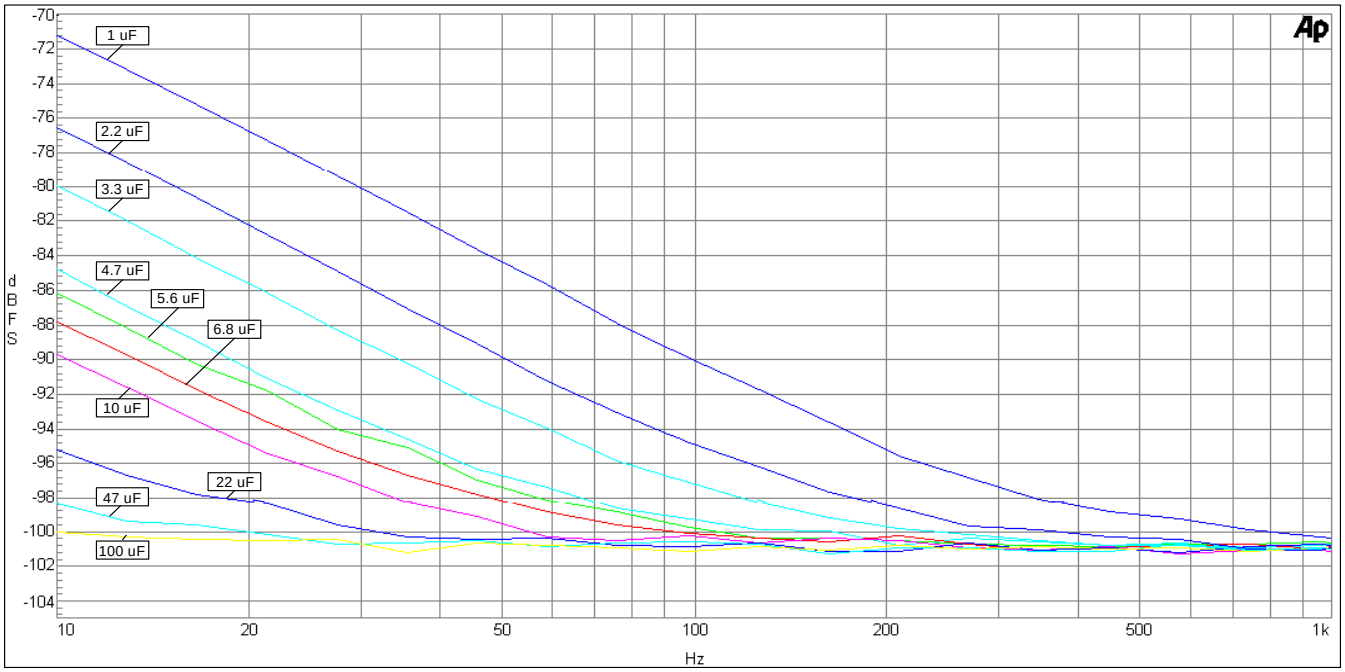


Figure 22. CS5340 THD+N versus Frequency

5. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

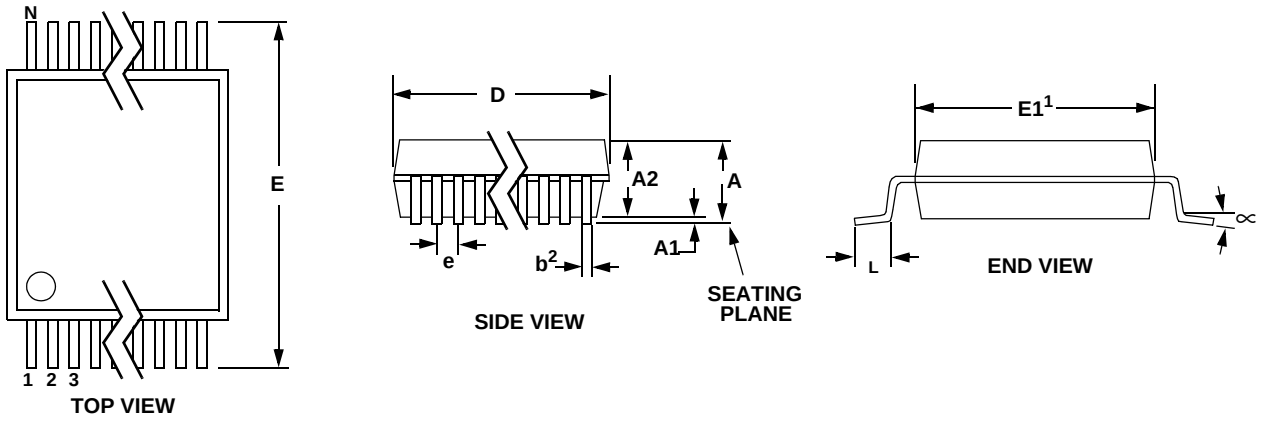
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

6. PACKAGE DIMENSIONS

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters

1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Junction to Ambient Thermal Impedance	θ_{JA}	-	75	-	°C/W

7. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS5340	101 dB, 192 kHz, Multi-Bit Audio A/D Converter	16-TSSOP	YES	Commercial	-10° to +70° C	Bulk	CS5340-CZZ
						Tape & Reel	CS5340-CZZR
CS5340	101 dB, 192 kHz, Multi-Bit Audio A/D Converter	16-TSSOP	YES	Automotive	-40° to +85° C	Bulk	CS5340-DZZ
						Tape & Reel	CS5340-DZZR
CDB5340	CS5340 Evaluation Board	-	-	-	-	-	CDB5340

8. REVISION HISTORY

Release	Changes
PP3	Remove CS5340-CZ from Ordering Information Redefine Serial Audio Port Switching Characteristics Correct dimension “e” under Package Dimensions Update Output Sample Rate Range
F1	Update maximum current and power specifications Update Filt+ output impedance specification
F2	Reduced minimum sample rate to 4 kHz for Double-Speed Mode 128x in Table 1 on page 15 Updated Legal Text

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com.

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER’S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER’S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS’ FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.