



Achieving Unprecedented Cost & Performance For Applications Requiring Multiplexed, High-Resolution ADC Functionality

*Leveraging New High-throughput Data Converters
With Superior Dynamic Non Linearity Performance*

*Overcoming the Design Limitations Associated with SARs
While Delivering Comparable High-Performance and Low-Latency
Along with Excellent Accuracy and Ease-of-Use*

Presented by
Cirrus Logic

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Overview

Analog-to-Digital Converters (ADCs) have long been a key linchpin element in the design and implementation of critical systems for many scientific, industrial, medical and consumer applications. With both product feature sets and performance demands continuing to escalate relentlessly, designers are always looking for more cost-effective methods to achieve the desired measurement results from their data converter circuits.

A widening range of complex designs, such as Automated Test Equipment (ATE), medical instrumentation and monitoring devices, data acquisition systems, laboratory instrument and Programmable Logic Controllers (PLCs) for industrial automation all depend on high-resolution ADCs in order to meet application objectives. In effect, it is the ADC that provides the link between the “real world” of analog phenomena and the “processing world” that uses digital information.

The fundamental requirements for ADCs always revolve around resolution, accuracy and bandwidth. Other important considerations that must be considered in selecting an ADC are signal-to-noise performance, distortion and latency. Many applications need rapid responsiveness from ADCs in order to process high-frequency or continuous readings from various sensors. The ability to efficiently multiplex multiple signals within the ADC is becoming increasingly important. This is due to the growing requirement to handle multiple analog inputs within the same device, such as designing PLCs that are able to simultaneously monitor and integrate real-time inputs from multiple sensors within a production environment.

Many conventional ADC architectures have inputs which present difficult drive requirements, demanding costly high-performance input buffers in order to deliver the needed responsiveness for continuous processing scenarios. In addition, some ADC architectures even impose “mandatory quiet time” in which the system can’t access the ADC’s output during the sampling process, further complicating the design task.

Of course, the other requirements that must be key considerations in any component selection include the cost of the device itself as well as the cost of any support circuitry required to assure its proper functioning within the overall design. This can be a particularly important issue with ADCs, especially when used in a high-performance multiplexed environment, because the required support circuitry can vary significantly depending on the type of ADC selected. For example, if the ADC architecture doesn’t inherently provide excellent noise rejection and measurement accuracy, it can necessitate over-designing the circuit in order to meet performance goals. In this regard, designs based on conventional successive approximation register (SAR) devices can present particular challenges because the board space, costs and power requirements associated with designing input buffers can quickly outweigh the apparent low-power specifications for the SAR itself. All of these factors play a critical role in the cost-effective achievement of design goals.

The Traditional SAR Approach

Traditionally, the types of high-performance applications mentioned above have been designed around ADCs using a SAR architecture, which provides a series of “snapshots” of the data at successive points in time. SARs generally have been targeted at applications that require fast response and low latency; however, because SAR devices are sensitive to noise and have relatively low DNL performance, the need for significant support circuitry often drives up the overall cost and complexity of SAR-based designs.

Poor linearity performance presents particularly challenging problems because this error cannot be averaged out by over sampling of the signal. In too many cases, design engineers must compensate by over-specifying the SAR and over-designing the system in order to make up for SARs’ poor DNL performance. Similarly, the higher noise sensitivity of SARs and limited noise-rejection capabilities present additional design challenges, especially in the inherently noisy environments for many deployments, such as PLCs on production floors or clusters of medical instrumentation in close proximity.

In contrast, ADCs using Delta-Sigma architectures have traditionally been able to deliver superior DNL and noise performance and allow for much less complex support circuitry. Until recently, Delta-Sigma ADCs have not been considered appropriate for use in high-performance applications requiring low latency and high conversion rates, to achieve wide signal bandwidth. However, as illustrated by the testing data in the balance of this paper, such “conventional wisdom” no longer holds true.

Introducing a New High-Throughput Delta-Sigma Architecture

With the introduction of the new CS556x/7x/8x family of gigh-throughput data Converters, Cirrus Logic has radically expanded the range of options available to system designers. Consisting of 16- and 24-bit ADC devices, the entire product family is built around an advanced high-throughput Delta Sigma architecture that is designed to fully settle on every conversion at rates up to 200 ksp/s. This provides high-response, low-latency performance that is comparable or better than SAR devices and therefore makes the new high-throughput Delta-Sigma devices ideal as cost-effective alternatives in applications that traditionally required SARs.

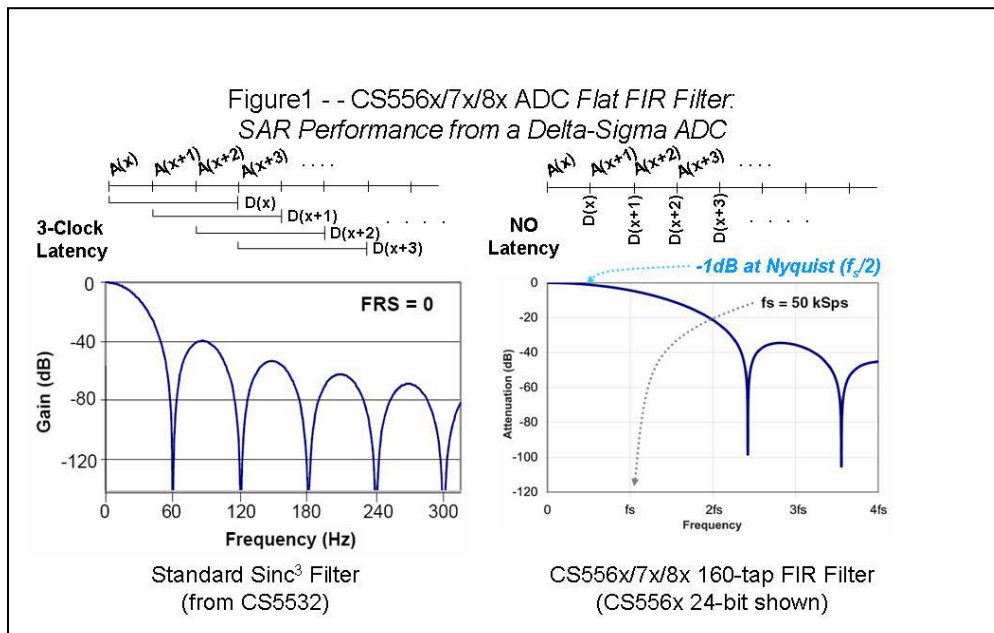
All members of the new product series incorporate the following key features:

- Buffered high-impedance inputs (single-ended or differential)
- 5V or $\pm 2.5V$ analog supply
- 1.8V, 2.5V or 3.3V digital supply
- Fully self-calibrating (for offset and gain errors over supply and temperature range)
- Flexible serial digital interface (master and slave modes)
- $-40^{\circ}C$ to $+85^{\circ}C$ operating range
- 24-lead SSOP package

All devices in the product family are pin-compatible, thereby enabling designers to smoothly proliferate a proven design into multiple product platforms with minimal redesign.

Single-Cycle Latency

In the past, Delta-Sigma-type ADCs have focused primarily on the highest-resolution measurement of slow-changing signals such as those from temperature sensors and weigh scale load cells. Since noise rejection is critical to obtaining measurement accuracy in noisy digital environments, designers have already become accustomed to seeing long “sinc”-type digital filters which feature excellent rejection of line frequency interference, such as 50 and 60Hz line frequencies and their harmonics. These filters are easy to implement, consume minimal die area and feature excellent noise performance. However such filters have tended to be quite long (large number of conversion cycles needed to process the input signal before delivering an output word) and thus are slow to respond to a change in the input. For example, the left side of Figure 1 illustrates the 3-conversion



latency of the digital filter used in the popular CS553x family of high-resolution ADCs.

The CS556x/7x/8x family incorporates a unique fast FIR-type filter that offers two major advantages. First, the filter is nearly flat to twice the sampling frequency, providing users with unrestricted frequency response, just as users have come to expect from SAR-type converters. Second, (as shown on the right side of Figure 1) the filter is processed quickly, and delivers a new output word after only one sampling cycle. *This single-conversion latency allows the new family to offer the excellent noise and DNL performance of a delta-sigma ADC with the high sample rate and Nyquist bandwidth of a SAR converter!*

Another key advantage of the new design is the ability to overcome the “quiet period” imposed by many conventional SAR devices, in which the ADC output cannot be accessed during certain parts of the sampling process. Testing of the CS556x/7x/8x family has demonstrated that accessing the digital outputs, at any time during the conversion cycle, has no impact on the performance of the device, including during full-speed operation.

Another important capability is the ability to convert on-demand (another SAR feature). This capability makes these devices ideal for conducting asynchronous measurements, which are often required in production environments. This allows for the ability to coordinate conversions with specific events, such as synchronizing flow with pulses or other sensor inputs. In addition, true bipolar inputs are available when running bipolar supplies. Current industry products run single-supply (+5V only) and require a level-shifter to move a bipolar signal up above ground, which weigh down the system error budget with additional gain and offset errors.

Buffered Inputs Provide Numerous Advantages

As has been discussed, SAR-type converters present numerous design challenges. Nowhere is this more apparent than at the analog signal inputs, where the designer must pay strict attention to component selection and circuit layout in order to obtain the measurement accuracy specified for the converter in the face of multiple noise sources. Considering that the SAR converter itself can be a major noise generator due to the high-speed comparator used in SAR architectures and the fast-changing digital circuitry within the device, this is often no small feat and often a daunting task for even the most experienced system designers.

In comparison, Delta-Sigma converters offer numerous inherent advantages which result in significantly improved performance due to low sensitivity to noise in addition to their inherently superior accuracy. First, this new family of devices provides integrated high-impedance input buffer amplifiers which make it very easy to achieve the full specified performance without complex, expensive external input buffer circuits. SAR-based devices usually utilize some type of sample-and-hold-type circuit to maintain a stable representation of the sampled input signal during the conversion. As a result, the inputs of these devices usually present a very low impedance to the signal source which usually includes a very large capacitance requiring an unusually robust amplifier circuit to maintain a stable level at the input to the ADC during the dynamic sampling period. This can be an extremely challenging design task, which in many cases demands buffer circuits which exceed the cost and complexity of the remainder of the converter circuit, as noise which is allowed to degrade the sampled input signal directly affects the accuracy of the conversion. On the other hand, in some applications, this new family of high-throughput Delta-Sigma-based devices can in some cases be driven directly from the sensor, without buffer amplifiers such as those required by conventional SARs.

Second, since they over-sample at the input, multiple samples (160 samples in the case of the 24-bit CS5560/1 devices, with samples taken at an 8MHz rate), the low-pass filter

provided within the Delta-Sigma Modulator loop and the mathematical averaging performed within the digital filter reject or even ignore much of the noise which creates such significant problems for SAR-based designs.

Another limitation often encountered in the current mixed-signal environment is the single-supply operation imposed by the use of low-voltage sub-micron CMOS process technologies. The new CS556x/7x/8x family of products goes the “extra mile” by offering true bipolar analog input capability when operating from $\pm 2.5V$ supplies. For users measuring ground-referred AC signals or transducers with negative-going outputs this is a significant advantage, as the circuit needed to shift a below-ground signal to meet the input requirements of the single-supply converter requires a level-shifting amplifier which introduces additional noise and offset error to the sensitive low-level signal.

The following sections provide detailed performance comparisons for critical parameters, such as Distortion Performance and Dynamic Non-Linearity.

Distortion Performance

Figures 2a and 2b show a comparison of the distortion performance for a widely used SAR device and the high-throughput Delta-Sigma CS5571 device. As can be seen, the CS5571 significantly outperformed the SAR device. At -12 dB of FS, the SAR exhibited a signal-distortion ratio of 91.6 dB while the CS5571 showed a 100 dB S/D ratio. One primary reason for the Delta-Sigma device’s better distortion performance is the superior code size uniformity as a result of its significantly better DNL performance (detailed in the next section).

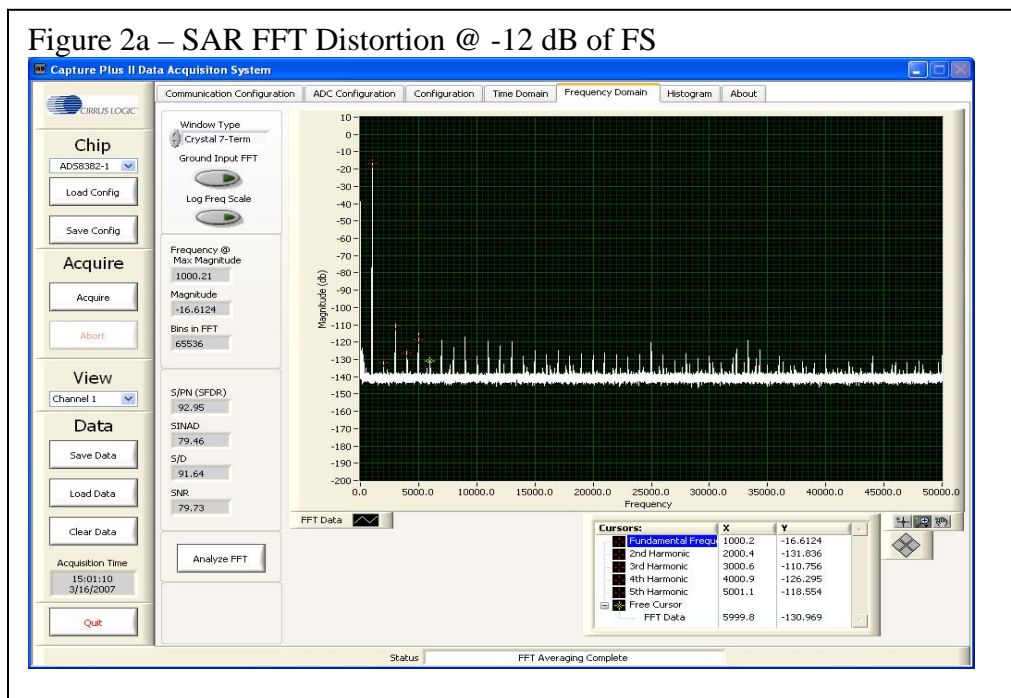
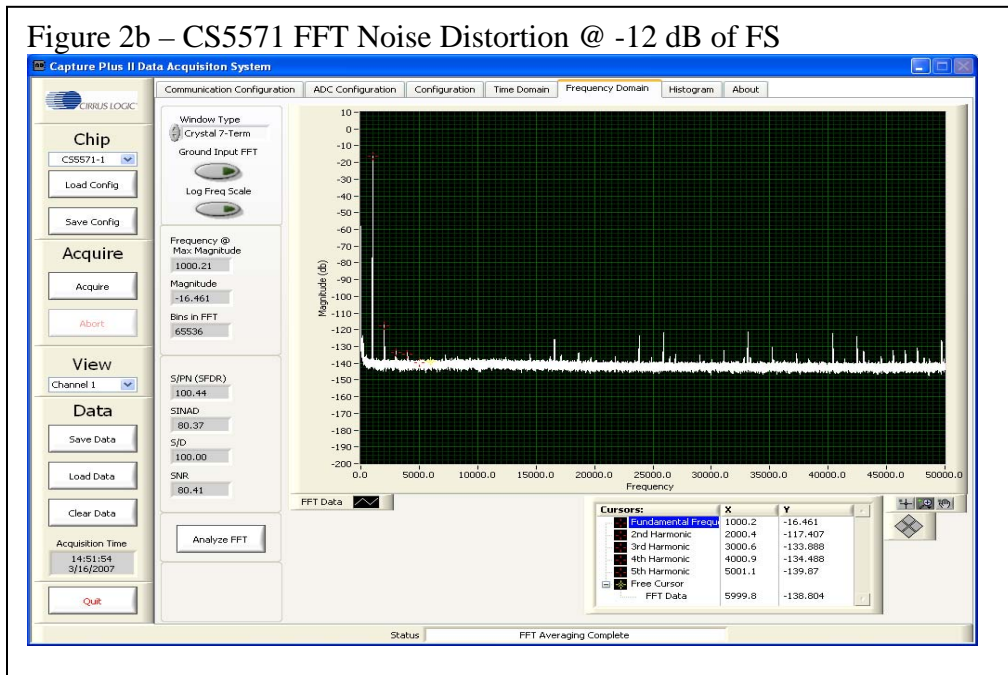


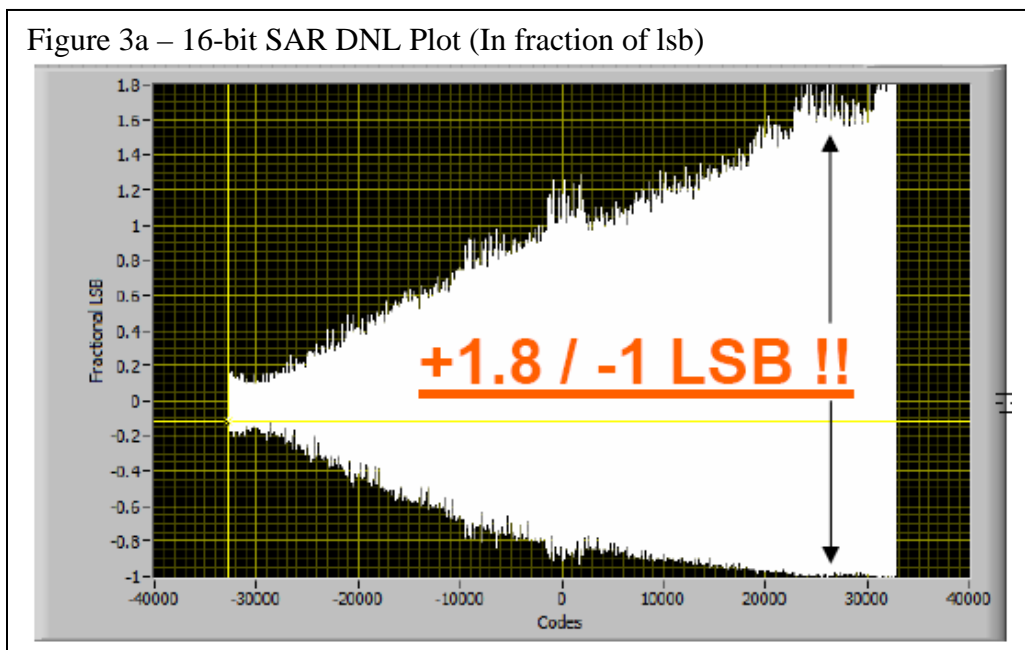
Figure 2b – CS5571 FFT Noise Distortion @ -12 dB of FS



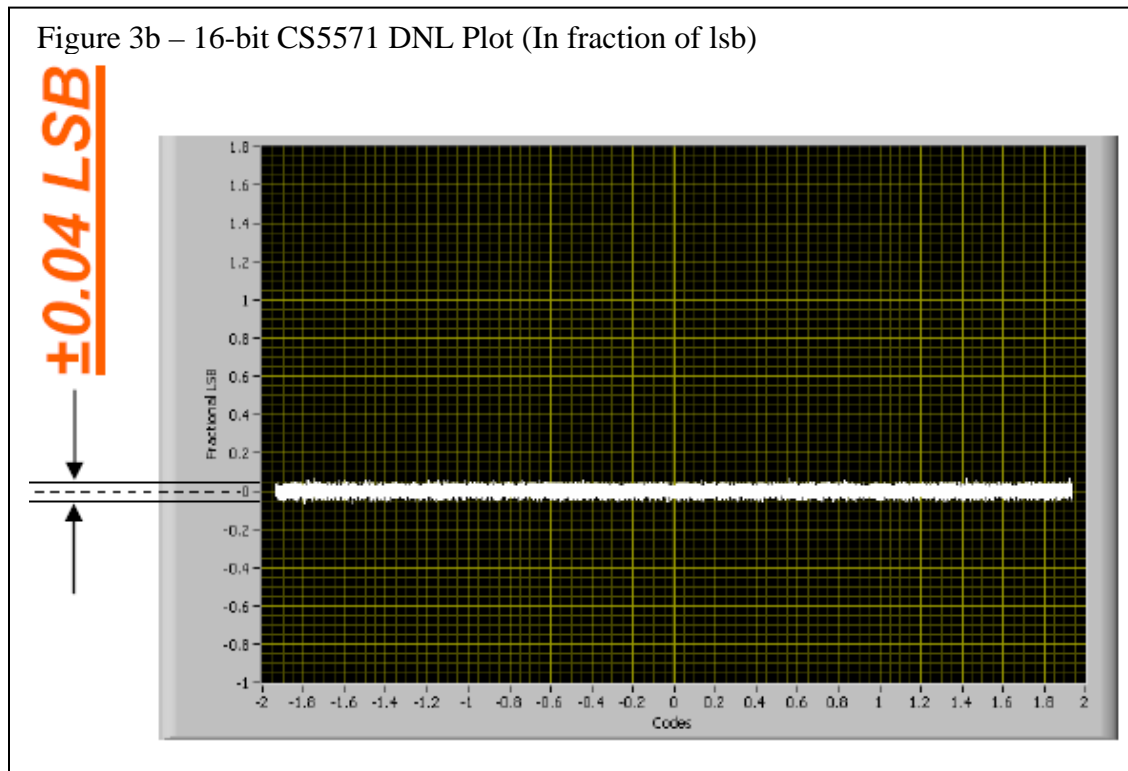
Dynamic Non Linearity Performance

DNL is basically the measure of code width variation, normalized to full scale. It is the deviation from a uniform or mean code size, which results in one code size representing a different voltage step size than another code. DNL plots, such as Figures 3a and 3b, provide a clear visual representation of variations in code size, which contribute to missing codes, gain and offset errors. As can be seen, the SAR DNL plot, measured from a competitor's leading SAR device, shows a wide variation in code size, while the

Figure 3a – 16-bit SAR DNL Plot (In fraction of lsb)



accompanying CS5571 DNL plot shows significantly lower error across the entire input range while running at the same conversion speed.



A Revolutionary Design – With a Long History of Excellence

It's important to also note that this new family of high-throughput Delta-Sigma devices comes from a supplier that already is recognized throughout the world for its expertise in developing high-precision analog and mixed-signal integrated circuits (ICs) for a broad range of consumer and industrial markets. Cirrus Logic's extensive product portfolio already includes analog and mixed-signal audio ICs for consumer, professional and automotive entertainment applications, as well as high-precision analog and mixed-signal ICs for Industrial applications, such as industrial measurement, analytical instruments, consumer utility, digital power meters and seismic systems.

With technology roots that go back to 1984 (as Crystal Semiconductor), the development of the new CS556x/7x/8x family of devices is an outgrowth of both our long history of developing leading-edge ICs *and* a philosophy of understanding the end applications and targeting new product development to solve real-world challenges. As a long-term, highly experienced supplier of both SARs and Delta-Sigma ADCs, Cirrus Logic is ideally positioned with the knowledge and the development capabilities to resolve the

shortcomings of each product category and to create a new family that delivers the best of both worlds.

Typical Application Scenarios

This combination of high resolution and unrestricted signal bandwidth allows designers to perform noise processing and filtering of signals that are tailored to their specific application requirements. Where applicable, this could even include adaptive filtering, in which a system can dynamically modify its filters to adapt to a changing environment, offering new capabilities that have previously been unavailable for high-resolution measurement applications.

One of the most exciting application areas that will be positively impacted by this new technology is the design of embedded capabilities for PLCs and process control systems. Over recent years, industrial automation environments have been moving toward a greater emphasis on decentralized control, using compact, multi-function solutions that can be adapted to handle a variety of real-time sensor inputs along with embedded intelligence and closed-loop responsiveness for implementing local decision loops. In too many cases, the poor DNL performance, noise characteristics and the need for additional support circuitry have limited the usability of SARs for implementing next-generation modular PLCs.

Introduction of high-throughput Delta-Sigma devices overcomes these hurdles, making it possible for designers of PLCs to build in high resolution and low latency while maintaining high measurement accuracy with a very consistent level of DNL performance. This is particularly important for real-time closed-loop applications where it is critical to maintain “no missing code” performance and avoid steps in the transfer function of the ADC which could result in “undefined” conditions in the control loop.

Automated Test Equipment represents another key application area, in which multiple simultaneous input streams often must be monitored and processed in real time. Here again, consistent DNL performance is essential for achieving accurate test results, especially when continuously monitoring test information over an extended period of time while watching for small and sometimes subtle signal variations.

In addition, for some ATE systems that are used to test and measure noise-sensitive devices, the inherent noise sensitivity of SARs could present an additional challenge by actually interfering with accurate test results. As mentioned above, designers often resort to using SAR-type converters with significantly higher resolution or speed than they really need, and average multiple samples in an attempt to get the desired system measurement accuracy. This new family of high-throughput converters, on the other hand, can be depended upon to deliver full accuracy with every reading, thereby totally avoiding the need for excessive resolution or sampling rates and the post processing of less-than-optimal results. In the ATE realm this results in higher throughput, which equates directly with lower test costs for the end customer. ATE applications also represent an area in which the adaptive filtering possibilities can offer interesting

advantages by allowing the test parameters to be dynamically adjusted during the testing process.

Medical instrumentation is another important market segment that can benefit from the new high-throughput data converters. Devices such as bedside monitors, blood analyzers, and other diagnostic systems have traditionally used 12- to 16-bit ADCs but many designers of these devices have already recognized the potential advantages of transitioning to higher resolution ADCs. This will enable them to digitize a transducer signal directly and then to perform signal gain and offset corrections in software, thereby improving both accuracy and analytic flexibility. The availability of new high-throughput Delta-Sigma devices in a pin-compatible family of 16- and 24-bit offerings means that medical device designers can now make a smooth transition to higher resolution without the risks of running into a dead-end or compromising future flexibility.

Weigh scales represent another key application arena, in which the need for highly accurate continuous measurements provides a vital role for implementing precision batch control and high-speed weighing functions. The actual production output can span a diverse range from heavy bulk products, such as concrete, to consumer products such as potato chips; however, the need for accuracy and fast response is critical to achieve quality and throughput goals. For example, the weigh scales used in processing bags of potato chips must be able to provide weighing accuracy to $\pm .01$ oz for sustained processing speeds as high as 3 to 5 bags per second.

Summary

Because every member of the new family of high-throughput data converters provides unprecedented DNL performance, designers have a broader range of choices for cost effective achievement of application objectives. In fact, since the 16-bit members of this family deliver excellent linearity and noise performance, users can in many cases utilize a lower-speed ADC than they have selected in the past and abandon the practice of averaging the multiple data samples they get from a noisy SAR device, as the performance of these new ADCs provides fully accurate noise-free readings with every conversion.

The advanced approach of this data converter architecture addresses the fundamental objectives of high resolution, low latency and high sample rate. Support for applications with continuous sampling requirements can be provided without either necessitating large input buffers and complex support circuitry or imposing undue restrictions on accessing the devices' output buffer.

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