

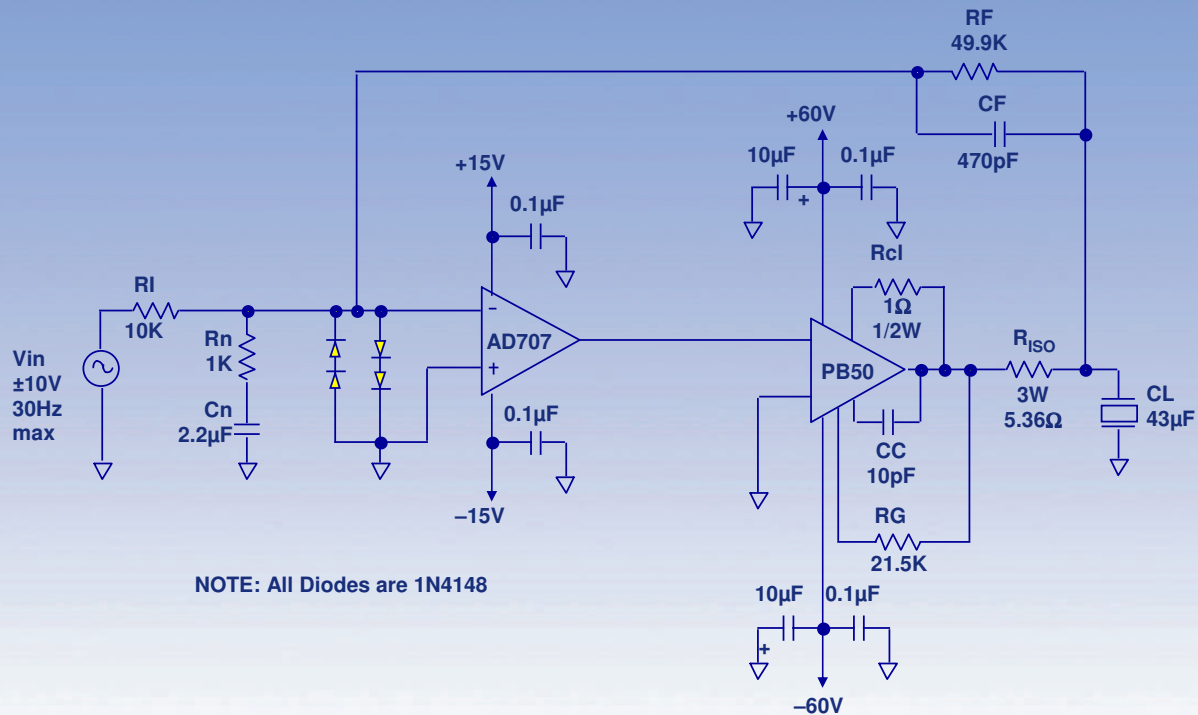


ATE APPLICATIONS

- High Voltage PPS
- High Current PPS
- AC Power Supplies
- Pin Drivers
- Waveform Generators
- Active Loads

There are an extensive array of applications for high power, high voltage, and/or high speed linear amplifiers in almost any type of automatic test equipment. Some of the most popular applications include different types of programmable power supplies. There are also ample opportunities for them to be used for waveform generation for DUT excitation.

LOW DRIFT PB50 PZT TESTER

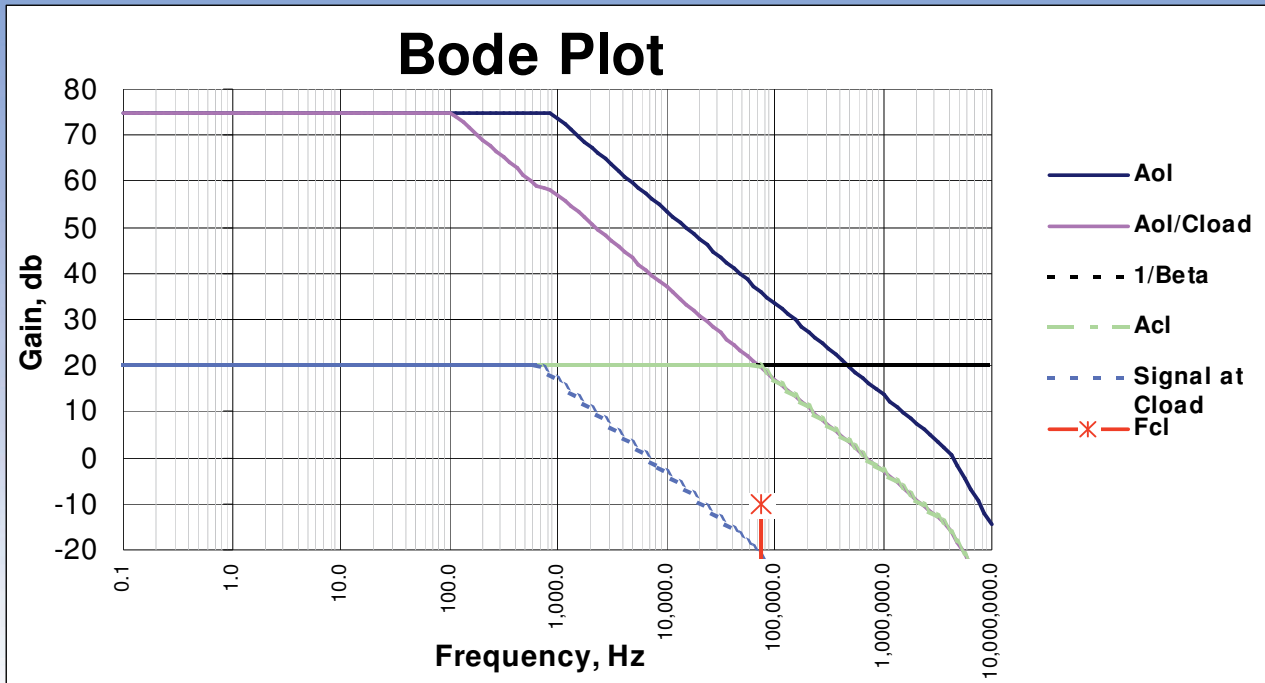


This Low Drift PB50 PZT Tester utilizes the flexibility of the PB58 power booster to provide low drift, high accuracy voltages to the PZT (Piezo Transducer) under test. The AD707 provides a composite amplifier input offset voltage of $90\mu\text{V}$, and a drift of $1\mu\text{V}/^\circ\text{C}$. Higher accuracy can be obtained with a different host amplifier or a better grade of AD707.

The PB50 is a versatile building block for ATE design that provides a low cost option for providing high voltages to devices under test. With supply voltages from $\pm 30\text{V}$ to $\pm 100\text{V}$, with a slew rate of $100\text{V}/\mu\text{S}$, and output current drive capability of 2A , The PB50 can provide up to 100KHz power bandwidth for high voltage test equipment. The composite amplifier approach for using this power booster allows the user to program the accuracy of the overall amplifier through selection of the front end host amplifier.

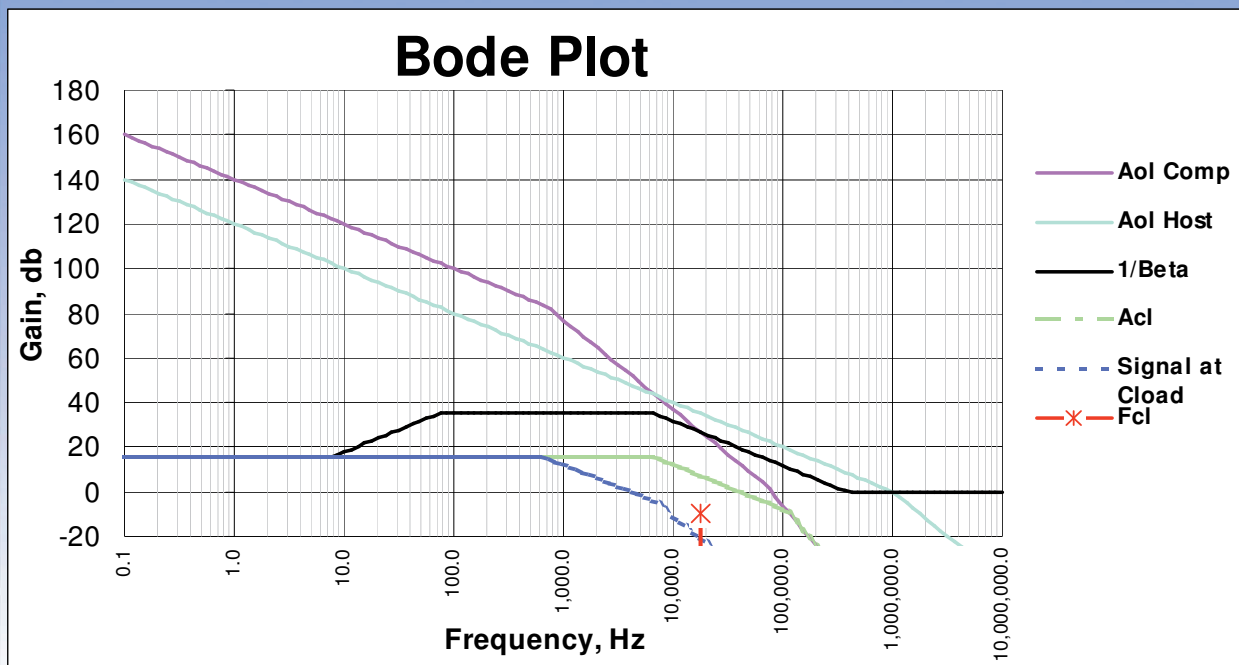
This particular implementation of the PB50 will present some stability challenges since we are driving a capacitive load with a composite amplifier. The approach to stabilizing this circuit will be to stabilize the power booster with its capacitive load and then stabilize the total composite amplifier. We don't stand a chance of stabilizing the composite amplifier if the output power booster is not stable first.

MAGNITUDE PLOT FOR PB50



Without the isolation resistor, the modified Aol curve would have changed to -40db per decade just under 1KHz giving an unacceptable intersection rate and about 2.5° phase margin rather than 90°.

COMPOSITE MAGNITUDE PLOT

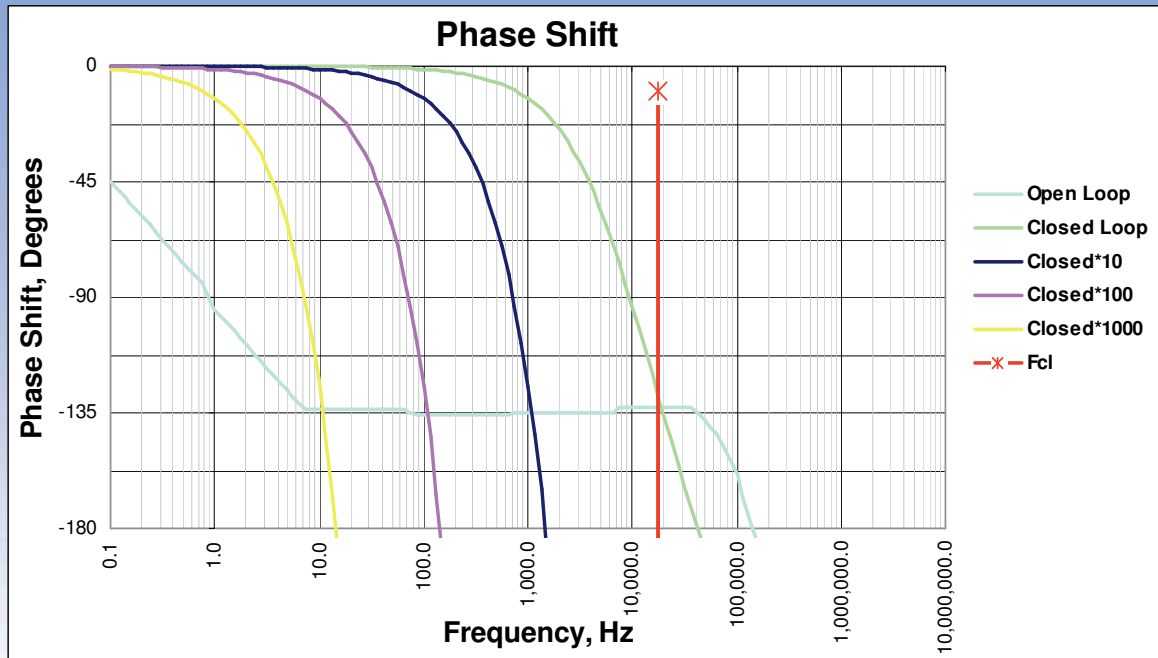


Now that the power stage is stable we add its closed loop gain to the open loop gain of the host amplifier. Note that it is the poles of the power stage rather than the host producing the -40db per decade slope in the area of interest. A roll off capacitor gives us required slope for good intersection rate and noise gain allows good placement of the actual intersection.

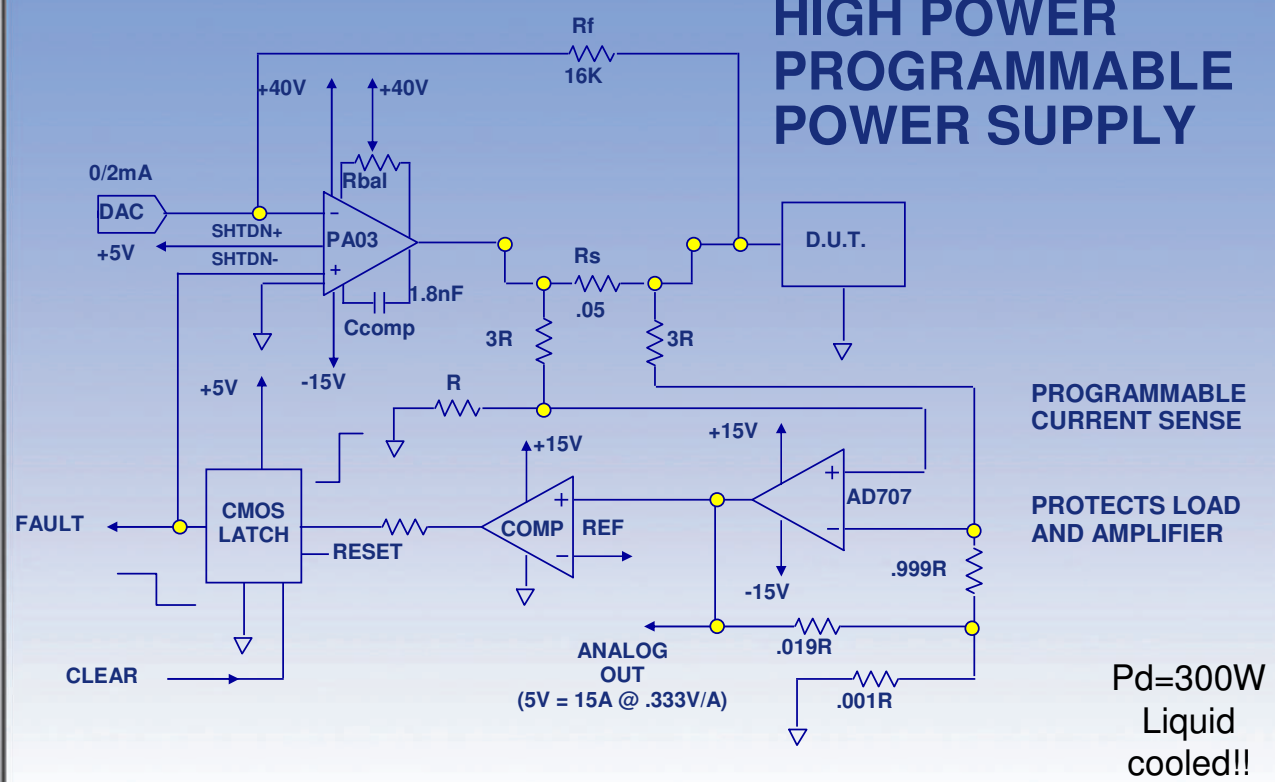
In this circuit final value selection was a result of playing “what-if”, and the phase component graph was very useful. The first pole of the host amplifier is at 0.1Hz giving a 90° open loop phase shift by 1Hz. The first pole of the power stage at just under 1KHz produced 180° at less than 10KHz. Visualizing the phase components moving on the graphs and using the R-C calculator make fairly short work of the design.



COMPOSITE OPEN LOOP PHASE PLOT

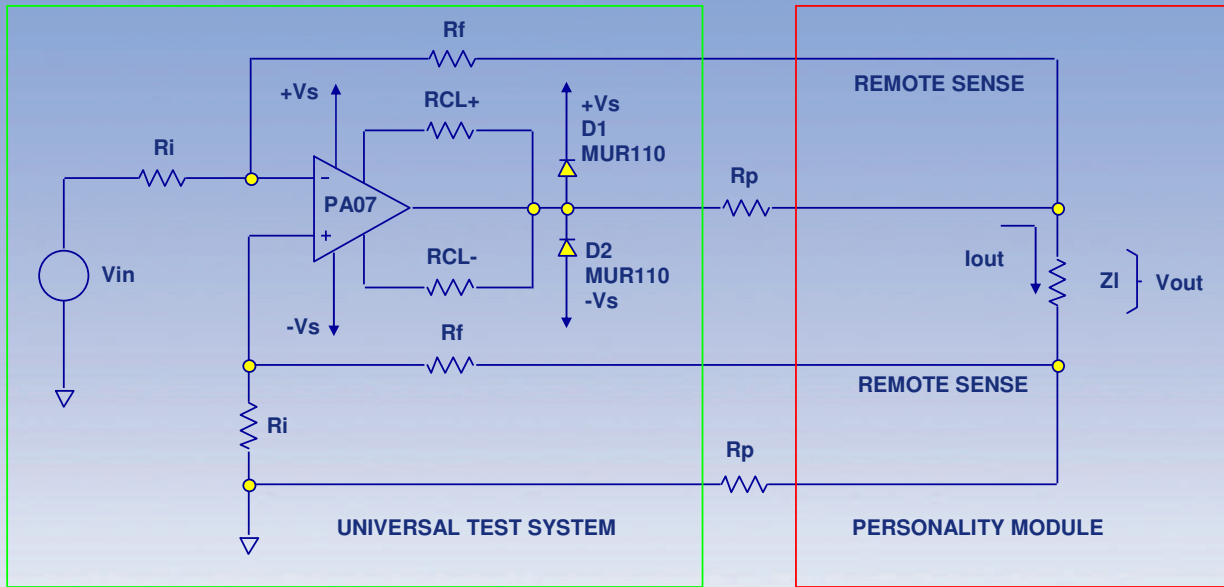


HIGH POWER PROGRAMMABLE POWER SUPPLY



In this circuit the PA03 is being used in a simple, reliable programmable power supply which utilizes the PA03 shutdown features. It requires little calibration because the current to voltage conversion of the DA converter output is done by the power op amp itself while a 12 bit DAC (i.e. DAC80) provided accuracy levels high enough to eliminate the need for adjustment. R_s senses current to the DUT. The AD707 is configured as a difference amplifier which senses the voltage across R_s and develops an analog output signal proportional to DUT current through R_s . It is then compared to a reference voltage which determines the current level desired. The comparator will trip high once this current limit is exceeded thus tripping a CMOS latch low and resulting in a 5V differential signal between the two shutdown pins on the PA03. This circuit is explained in detail in Application Note 6 in the Apex Data Book.

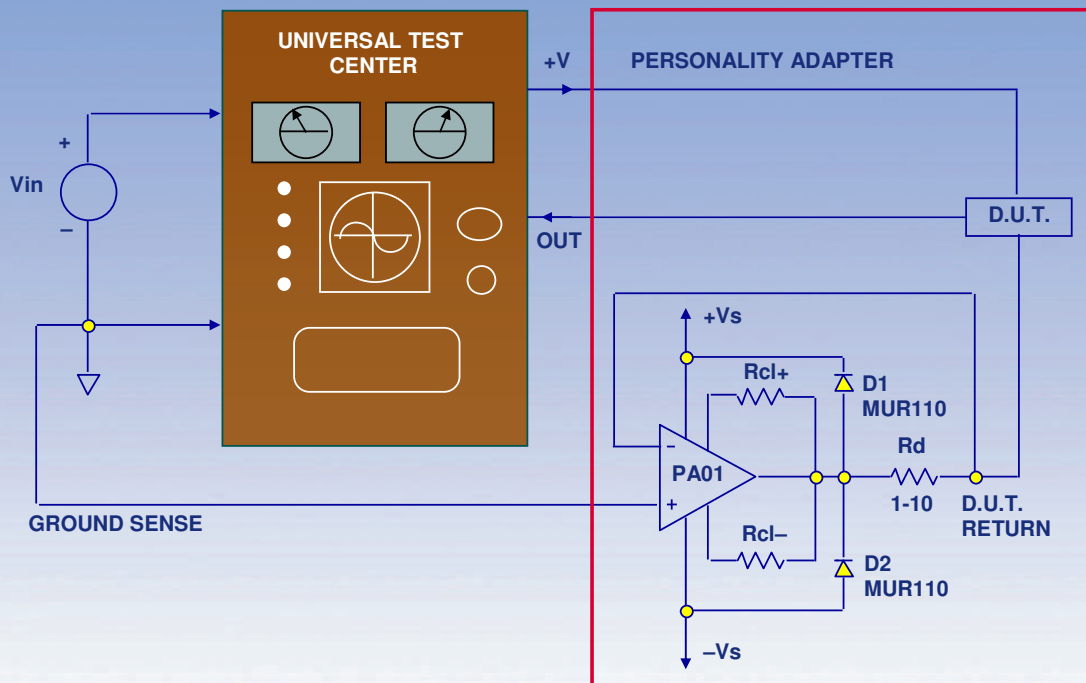
REMOTE SENSE



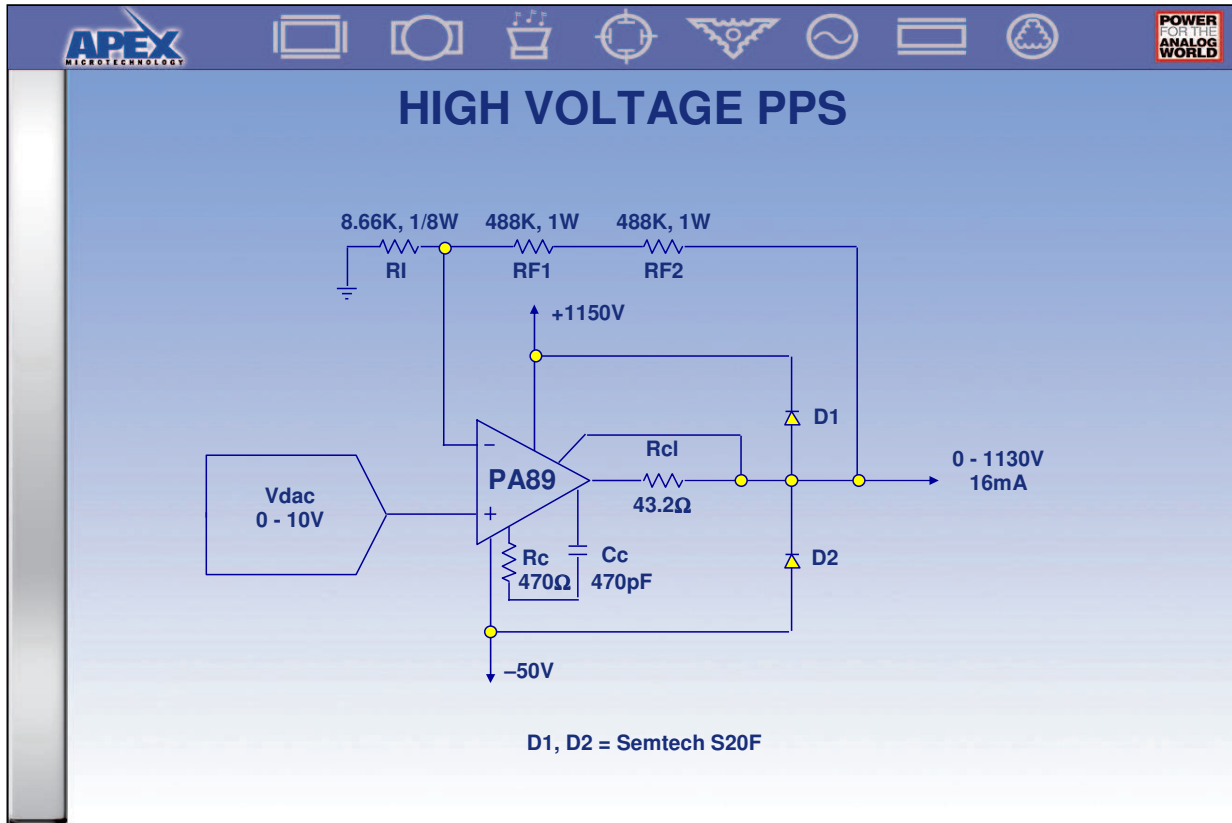
Universal test stations often contain a power op amp that is used to provide power to some remote load. If significant amounts of current are being delivered to this remote load, the parasitic resistance of the wiring can contribute significant errors to the measurements. For instance, 50 milliohms of wire resistance in the output and return line would result in an error voltage of 500mV with a 5A load current. When the power amplifier is configured as a differential amplifier, with the differential plus remote sense and minus remote sense lines being run directly to the load and connected across the load at the remote site, drops from the parasitic resistances become common mode signals to the difference amplifier and are rejected due to the high CMRR of the amplifier.

Ref. AN7

DRIVEN GROUND



Often a test rack is located quite a distance away from the actual test head where the DUT is being excited, or where measurements are being made. When the equipment at the personality adapter or the test head dumps a significant amount of current into a ground return line, enough voltage may be developed between the personality adapter and the universal test station to contribute significant errors to whatever measurements are being made. One way to solve this problem is to eliminate current flow in the ground line. This circuit accomplishes that feat by taking the reference ground from the universal test station and running a "ground sense" line over the personality adapter. This line is now used as a reference voltage input to a unity gain follower — in this case the PA01. The PA01 is used to generate a "remote ground." Now the ground current from the DUT or remote test equipment is dumped into the output of the PA01 where it is returned to one of the remote supply lines. The 1-10 ohm series resistor is used to keep power dissipation outside of the amplifier and have it dissipated in the resistor instead. Its value should be chosen such that the I_{max} (ground current) $\times R_s = V_o$ max of the PA01.



This high voltage programmable power supply utilizes the full voltage capability of the PA89. It uses asymmetrical power supplies to eliminate the necessity for biasing up the front end input DAC voltage to comply with common mode voltage requirements of the PA89, as well as providing adequate voltage headroom at the output so it can swing down to zero.

Although the PA89 can be used single supply, it ends up requiring large value resistors and high wattage resistors to bias the front end to comply with the input common mode voltage specification of $\pm V_s - 50$. The output would only be guaranteed to swing within 20 volts of ground. Asymmetrical power supplies, as discussed earlier, eliminate both of these problems.

With the current limit set at 16mA the PA89 can withstand a fault condition of a short to ground on the output by using an Apex HS06 heatsink, a TW05 thermal washer, and in a 25°C ambient environment, free air convection cooling.

Although the PA89 generally works at low currents ($< 60\text{mA}$), power dissipation is still a major design consideration due to the high voltage (remember $P = V \times I$).

As a high voltage amplifier the PA89 does present some unusual design considerations. The following is a quick check list of support components requiring special attention:

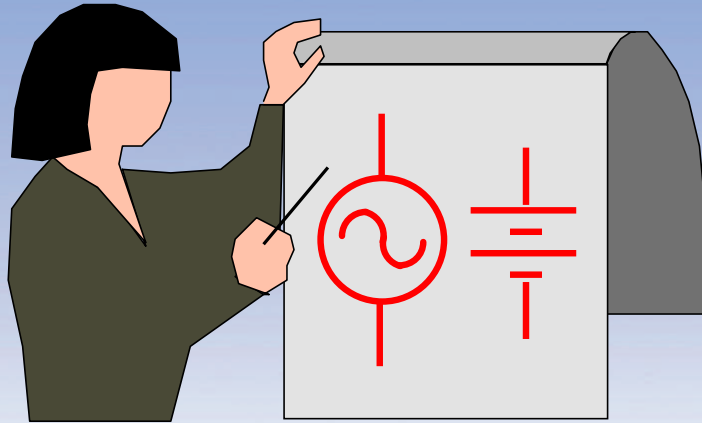
1) C_c —Compensation capacitor will see nearly the full supply voltage. In this case 1200V. Because of corona effects and partial discharge, this capacitor must be rated at twice the total supply voltage. Lower ratings can cause amplifier destruction.

2) R_{F1} and R_{F2} —Feedback resistors must be selected for power dissipation, voltage coefficient of resistance, and voltage breakdown rating.

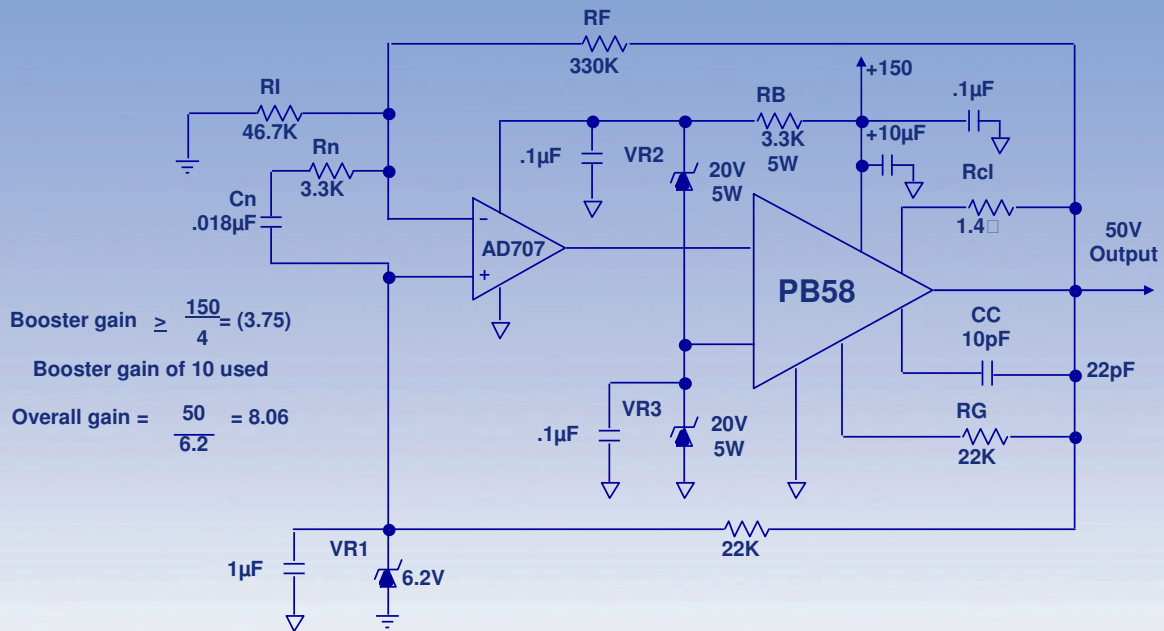
3) $D1$ and $D2$ —Flyback diodes must have a peak inverse voltage rating of the total supply voltage. Here we need a 1200V PIV rating minimum.



SOURCES



VOLTAGE REGULATOR WITH PB58



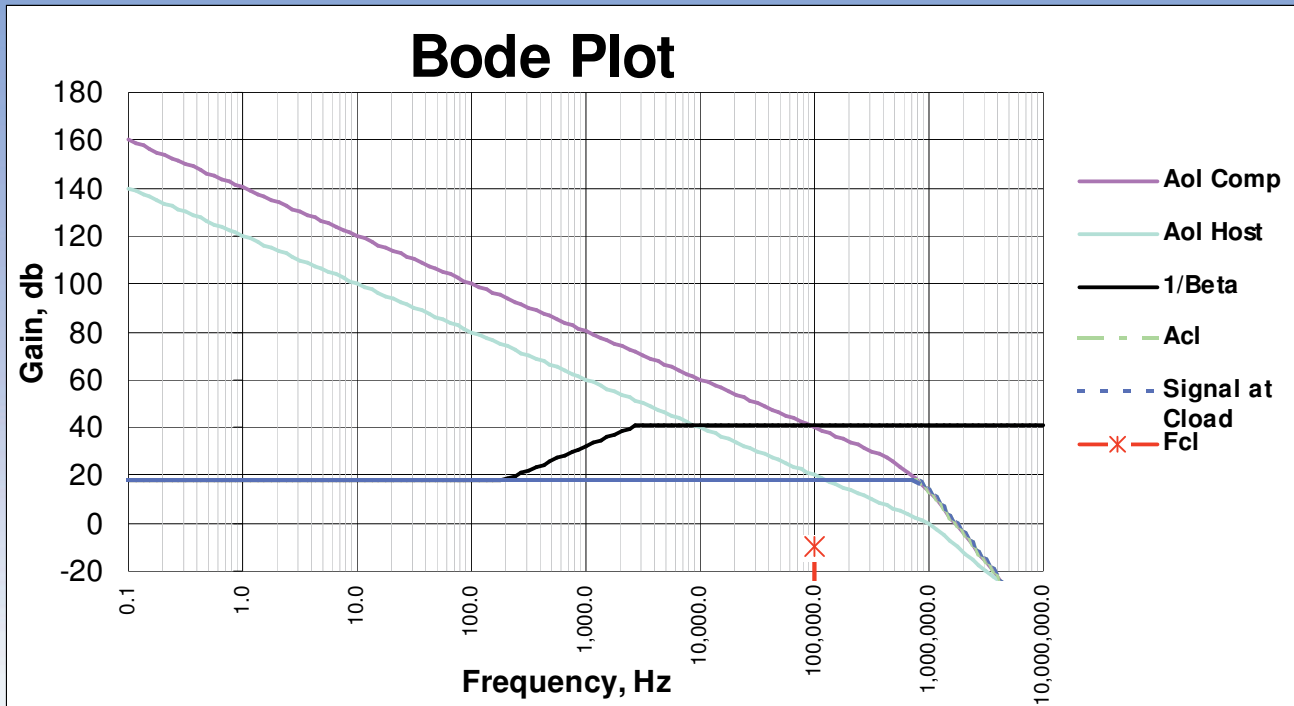
At first this may not seem to be the least costly approach to voltage regulator design. However, there is no packaged solution to regulating 150 volts down to 50 volts while being able to provide up to 500 mA (PB58 is rated up to 2A, but SOA limits us to 500 mA in this application). This regulator has both good source and good sink regulation characteristics.

This application does serve well to illustrate PB58 design techniques, and some of the limitations to be aware of. For instance, in normal applications the negative supply of PB58 must be 15 volts more negative than ground. In this application we have created a quasi-ground at the junction of VR2 and VR3 which meets this requirement. VR2 and VR3 also provide regulated supply voltage for the driver op amp.

The reference zener source is derived from the output of the regulator to improve supply rejection. The overall gain is whatever is necessary to multiply the 6.2 volt reference VR1, up to the required output voltage. In this case a gain of 8.06 for a 50 volt output. In the next few slides, we'll discuss stability considerations in the booster application.



COMPOSITE MAGNITUDE PLOT

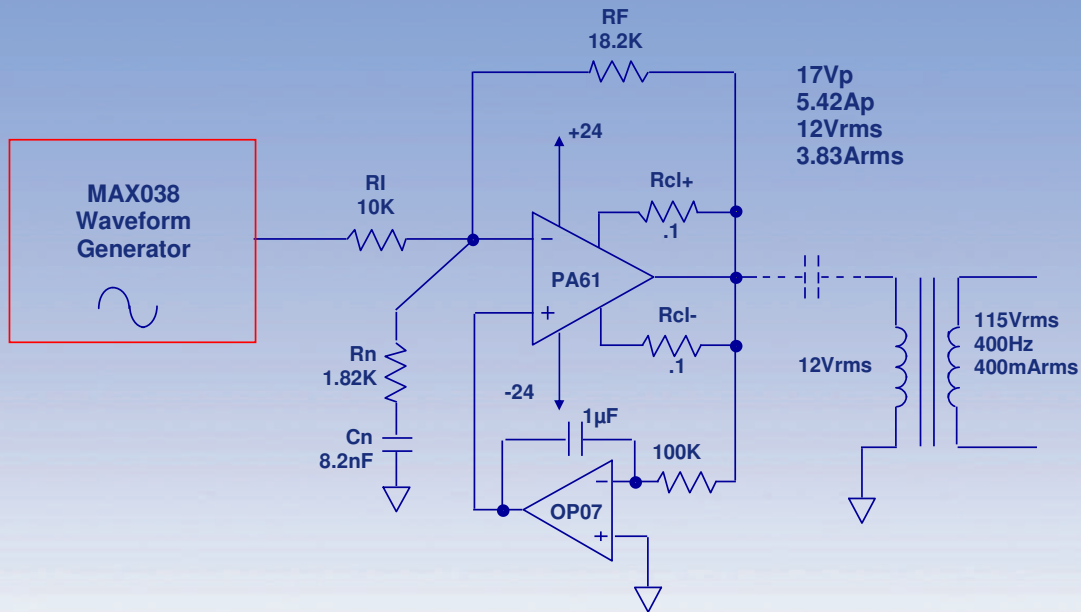


This circuit is not battling capacitive loading or inductance in the feedback path and each part of the composite would be stable on its own but the composite open loop gain reaches a slope of -60db per decade before crossing 0db.

While a DC gain of 100 (A short in place of C_n) would have made the circuit stable, the DC errors due to offset and drift would have been objectionable. Including C_n keeps DC gain at the desired level and produces a stable circuit.



400 Hz SERVO SUPPLY



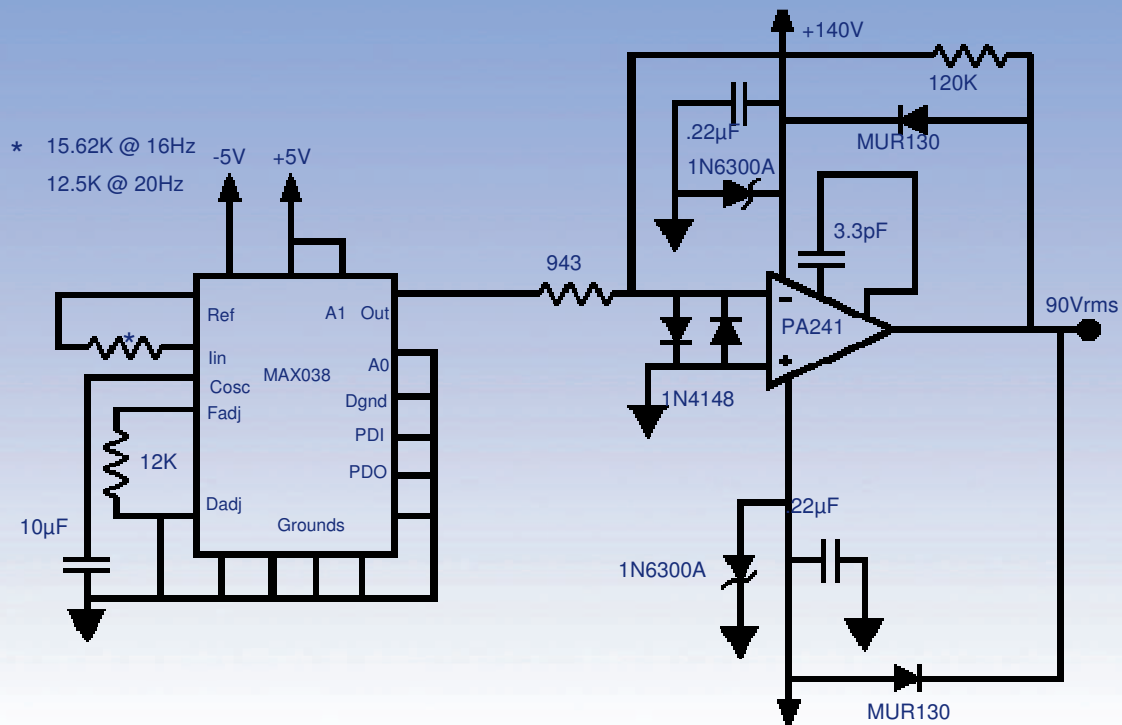
This 400Hz servo supply uses a separate oscillator to maintain oscillator stability under varying load conditions. The PA61 provides a gain of 1.8 to match the output of the industry standard 8038 waveform generator IC to the primary of a 12V to 115V step-up transformer.

The input R-C network is selected to provide unconditional stability on the PA61 with a phase margin of 45° in the 100Hz to 3kHz region. Phase margin increases to 90° at the 100kHz small signal bandwidth of this circuit. This extra phase margin allows for parasitic cable capacitance and/or capacitive loading on the output of the PA61 with guaranteed stability. The capacitor is selected for a corner frequency of 10KHz since this is well away from the 400Hz signal yet low enough to control any stability problems.

Note that the power supply is set to a value just large enough to accommodate the signal amplitude plus the amplifier's worst case output voltage swing specification. The use of minimum power supply voltage minimizes dissipation and improves efficiency.

If AC coupling should lead to unmanageable size bipolar capacitors, use an integrating amplifier (OP07 in this example) to compensate for offset voltage.

LOW POWER TELEPHONE RING GENERATOR



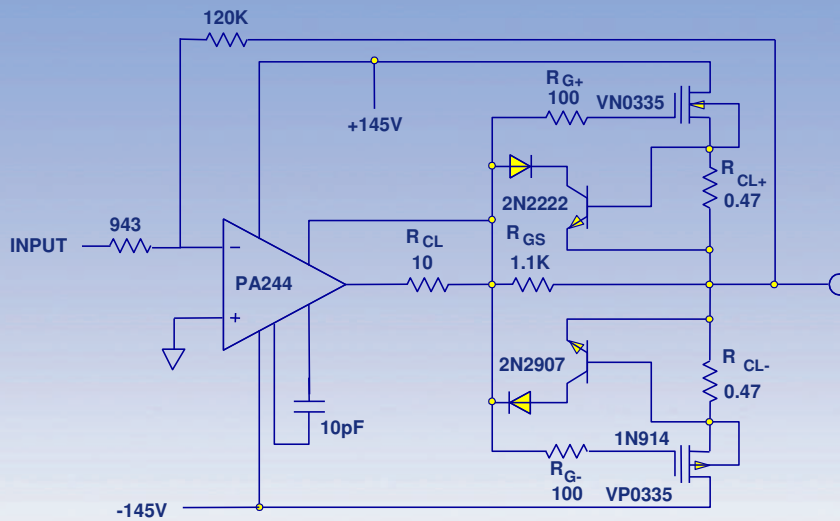
The MAX038 provides a 2Vp-p low distortion output signal. The PA141/142/144 is set for a gain of 127, boosting the overall output to 90Vrms. The recommended compensation for gains above 30 is used. If capacitive loading is at least 330pF at all times, the recommended snubber network may be omitted. The 27Ω resistor sets current limit to a nominal value of 111mA to insure peak currents of at least 88mA or 5.6W delivered to the load. This places total power dissipation at 3.8W, a level easily handled by the PA141 or P1A42. Unless exotic heatsinking methods are employed, the PA144 is typically limited to about 2W. The 3.8W figure assumes resistive loading and ignores the possibility of a shorted output. Power levels must be reduced if reactive loads or shorted loads are to be encountered.

The MUR130 diodes shunt any energy on the output to the supply rails which are in turn protected against overvoltage transients by the IN6300A transient voltage suppressors.

With the high voltage stage being a simple inverting circuit, it is very easy to scale the output down or up to 115Vrms. Summing in a DC offset could be done just as easily.

Ref. PA144 DATA SHEET

HIGH POWER TELEPHONE RING GENERATOR



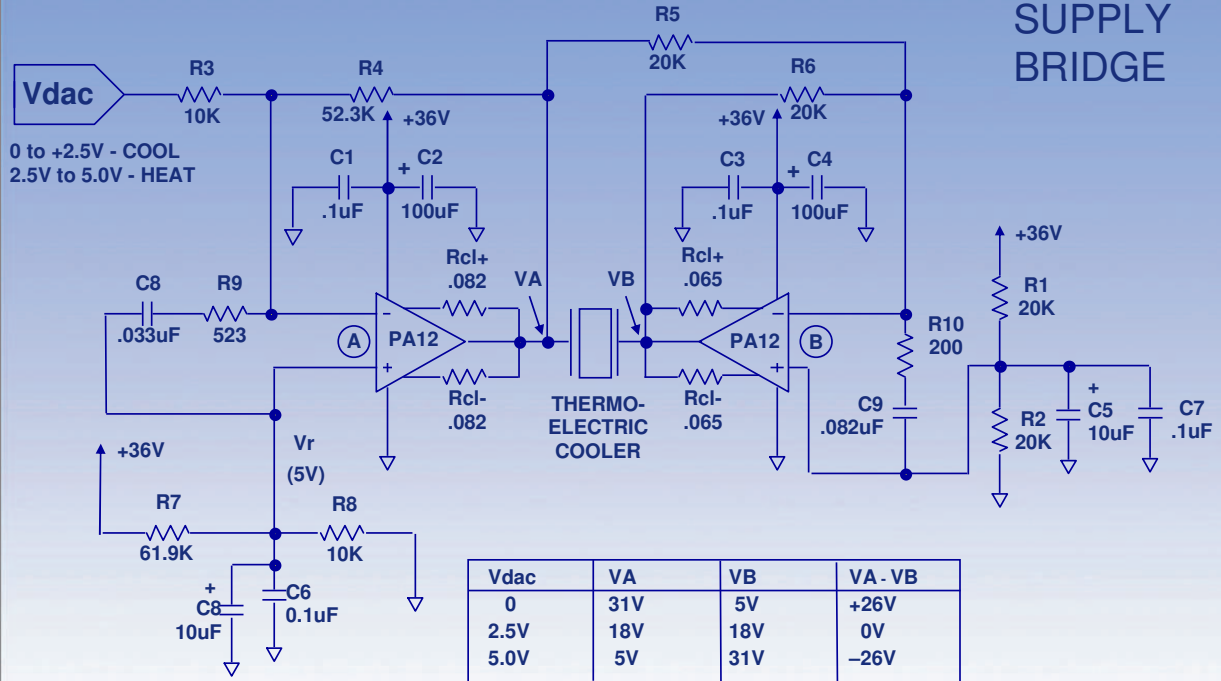
The signal source, protection requirements, and the basic operation shown here is the same as in the low power ring generator. Power supply bypassing and the use of a star grounding become much more important as power levels increase. To enable the ringing of more lines, external MOSFETs have been added. The choice of specific MOSFETs is determined entirely by current, voltage and power dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages or transconductance. Note that each MOSFET must be rated to handle the total supply voltage, 300 volts in this case.

Current limits have been set to a nominal of approximately 1.4A. Allowing for a 20% tolerance insures outputs of 1.1A pk or 0.78Arms. At 90Vrms, output power will be 70W and the peak dissipation requirement for each MOSFET will be 45W. At typical ringer frequencies the MOSFETs need to handle the 45W. Thermal averaging of the heatsink allows designing for 45W for the total amplifier or 22.5W per MOSFET if using multiple heatsinks.

The current limit resistor sets the PA244 current limit to approximately 9mA. This current flowing across R_{GS} limits drive voltage on the MOSFETs to 10V. Worst case power dissipation in the PA244 will then be 1.3W due to output current plus .6W due to quiescent current totaling 1.9W. Unless you are willing to cut holes in the PC board to contact the bottom of the surface mount package with an air or liquid cooling system, this is about the limit. Typical operation will generate less than 1W in the op amp. Replacing R_{GS} with a bi-directional zener will allow a cooler running op amp at the cost of increased distortion.

THERMO-ELECTRIC COOLER

SINGLE SUPPLY BRIDGE



- $V_{out} = V_A - V_B$
 $MAX V_{out} = +V_s - V_{satA} - V_{satB}$
 $= 36V - 5V - 5V = 26V_p$
- $Gain = V_{outpp}/V_{inpp} = (V_A - V_B)_{pp} / V_{inpp}$
 $52V_{pp}/5V_{pp} = 10.4$

Gain = $2 R_4/R_3$ since we have a bridge configuration.

The voltage gain across the load is twice that of the master amplifier, A, since +1V out of the amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +18V.

Therefore $R_4/R_3 = 5.2$

- Offset
 $V_A - V_B = +V_s(2(1 + R_4/R_3) \frac{R_8}{R_7 + R_8} - 1) - 2(R_4/R_3)V_{dac}$

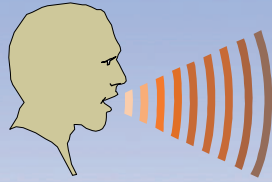
But when $V_{dac} = 0$ then $V_A - V_B = +26V$

Using $R_4/R_3 = 5.2$ and solving above yields $R_7 = 6.2 R_8$

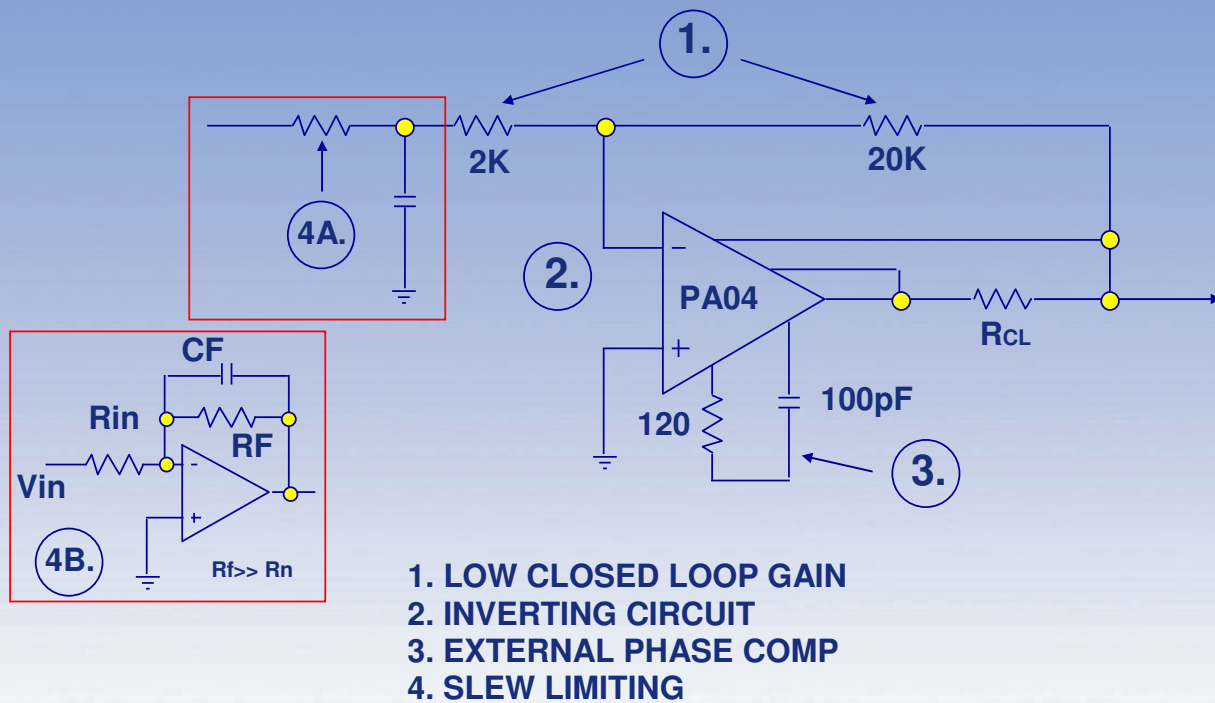
Choosing $R_8 = 10K$ implies $R_7 = 61.9K$

- Check for common mode voltage compliance:
 $5V$ meets the minimum common mode voltage spec.

AUDIO



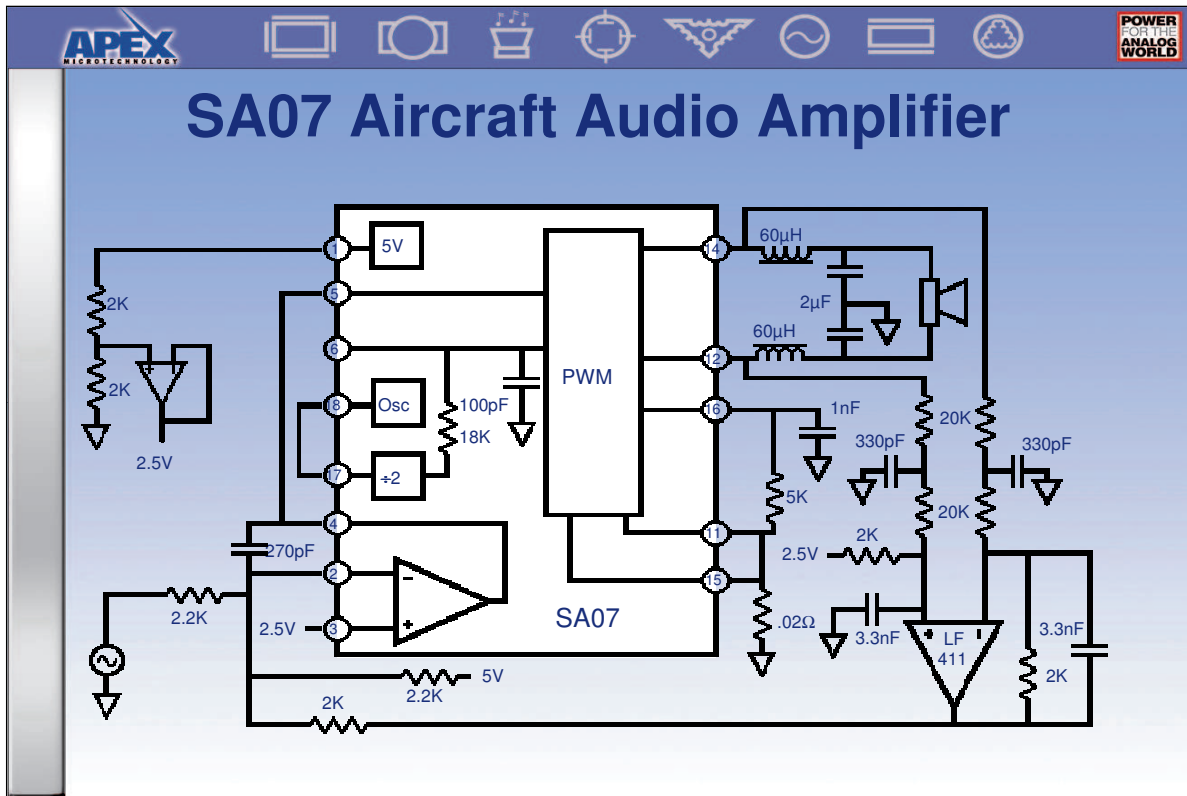
WIDE BAND - LOW DISTORTION DESIGN



When audio or ATE applications demand the best in distortion and bandwidth, there are four basic rules to follow:

1. Low closed loop gain insures maximum reduction of distortion because of increased loop gain. However, the heavy negative feedback can cause transient response problems during rapid transitions (slew rate overload). Rule #4 will show how to solve the transient response problem.
2. The inverting configuration, by forcing both inputs to 0 (remember your basic op amp theory), eliminates common mode signals and the errors (read: nonlinearities) that they cause.
3. External phase compensation allows the designer to tailor the circuit to the minimum acceptable compensation. This increases high frequency loop gain to further reduce distortion, especially at high frequencies. Consider noise gain compensation to improve stability for low gain and small compensation capacitors.
4. Input slew rate limiting (4A) designed to keep input signal transitions within the slew rate limit of the amplifier will eliminate transient overload problems. 4B) You may use an integrator to accomplish this function, while R_F/R_I pre-amplifies the input signal to accommodate a low power stage gain. Then $C_f = V_{in}/R_{in} \cdot A_{cl} / SR$.

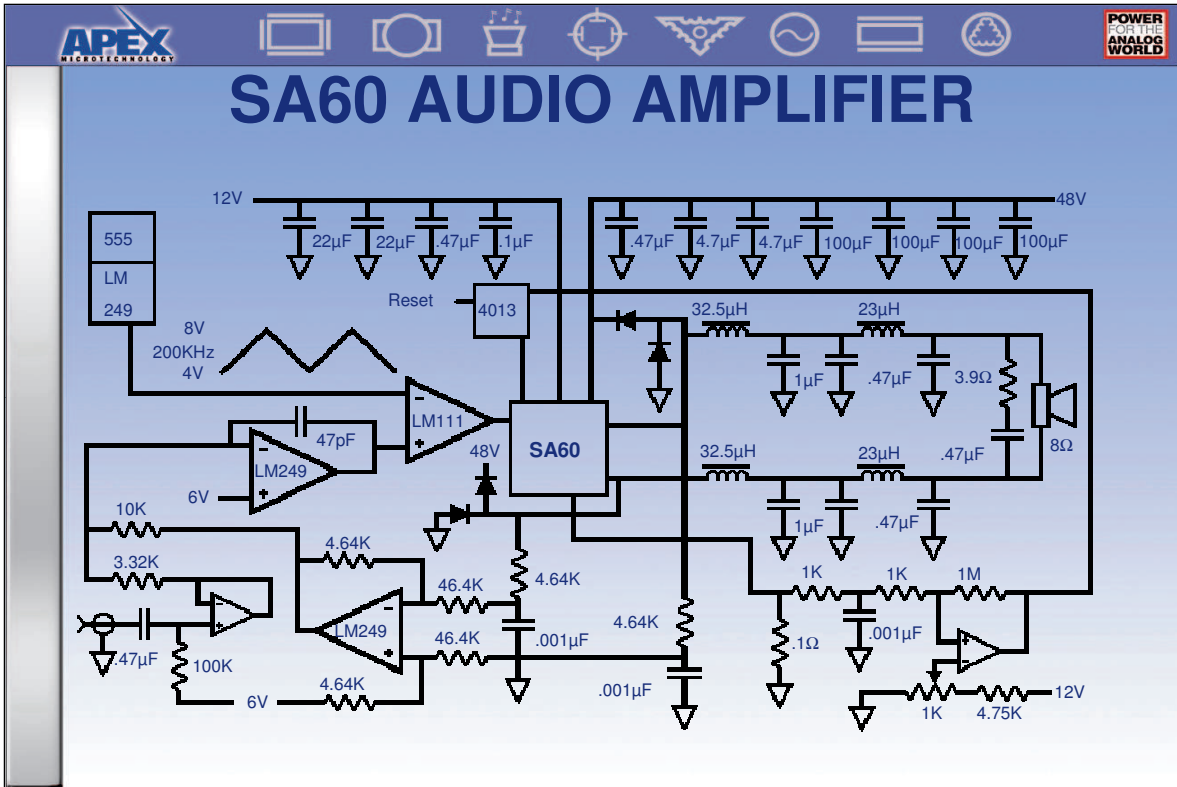
Ref. AN17



Weight is right at the top of the list of things airliners don't want. This is where the SA07 becomes the best choice for cabin audio. Heatsink concerns make PWM a natural choice and 500KHz switching cuts down the size of capacitors and even more important, the inductors. Not only is size and weight for a specific inductance reduced compared to a lower switching frequency, but having a wider band between switching and signal frequencies yields a filter with fewer components (a lower order filter). The filter is based on Power Design recommendations given 28V supply, 15KHz signal bandwidth and maximum ripple of 25mVpk.

The differential voltage amplifier has two poles at about 23.5KHz, a gain of 1/20 and the output is referenced to 2.5V. The integrator amplifier is also referenced to 2.5V and scaled to 1Vrms inputs which are ground referenced.

While not shown here, make no mistake about it, selection of bypass capacitors and careful layout make or break this application. In addition to 10µF per ampere low frequency bypass, use lower value ceramic chip capacitors to achieve low ESR well into the MHz region.



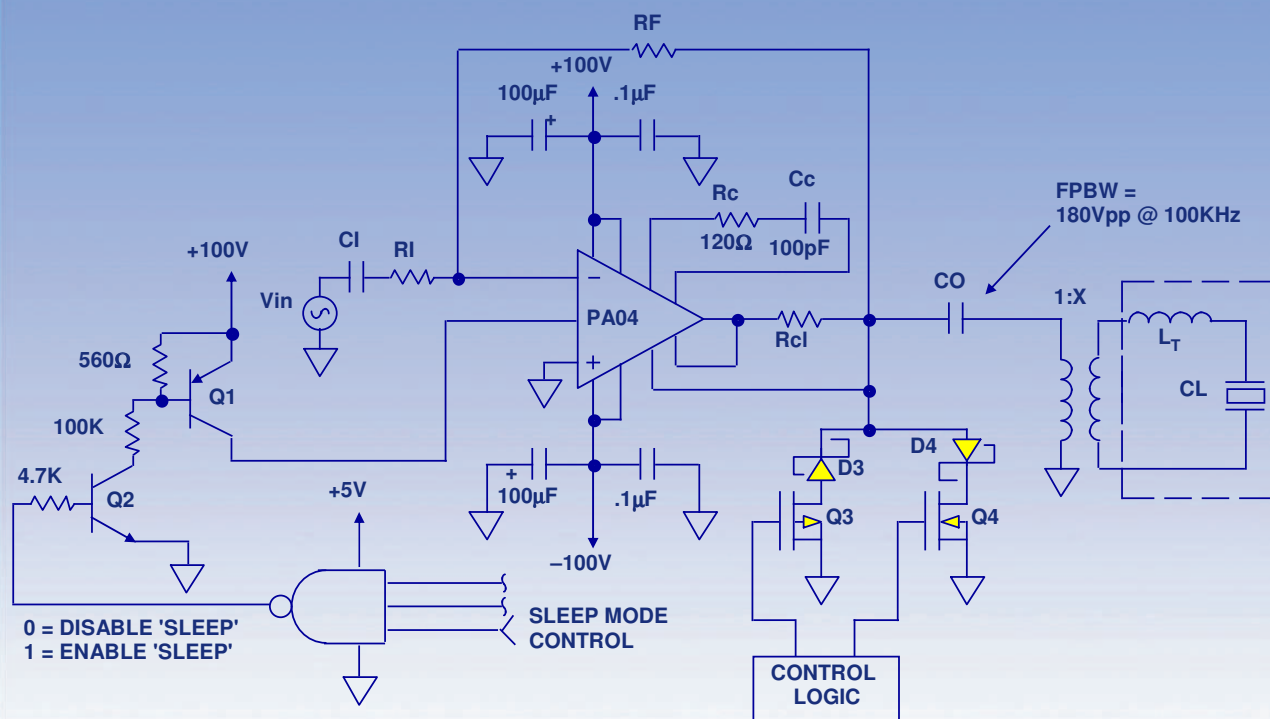
This class “D” audio amplifier is cost effective, cool running, good sounding and delivers up to 100W. Does any one know what this number would be if you bought the equipment as consumer audio gear?

Tested efficiency of this circuit was 80.6% at 60W output, meaning 14.4W wasted. A theoretical linear power stage would dissipate 72W delivering the same output from $\pm 48V$ supplies. Again, roughly that 5:1 heatsink savings of PWM over linear.

Operation of the overall circuit is similar to previous voltage output designs except there are more functions external to the PWM amplifier. The LM111 generates the PWM duty cycle based on the 6V referenced ramp and input signals. The SA51 converts this to power pulses. The filter removes most of the 200kHz switching frequency for the speaker. The differential amplifier also converts power pulses to an analog feedback signal. Over current is detected and latched to disable the power stage. Response time in the area of $5\mu s$ is required.

Capacitor arrays seen decoupling the supplies are not overkill. Larger values do a good job at lower frequency, lower values keep ESR low at the high end. Select capacitors specified for high current switching applications.

SONAR TRANSDUCER DRIVE



High current drive capability and wide power bandwidth make the PA04 ideally suited for sonar drive applications.

Often the amplifier is required to drive the primary of a transformer to step-up its output voltage to a desired high voltage for end drive to the sonar transducer. Because transformers do not work well when saturated it is essential to minimize DC current flow in them. AC coupling of the input signal and/or the output minimizes and/or eliminates the DC input offset voltage of the PA04 from becoming gained up by the gain of the amplifier, creating a large DC offset at the output.

Often times, either through the construction of the transformer or through an additional inductor, L_T , the sonar transducer, predominantly capacitive by nature, is tuned to look resistive for a narrow band of frequencies. This minimizes SOA stresses on the PA04. It is a good idea however to consider worst case capacitive loading reflected to the primary of the transformer onto the PA04 for AC stability considerations, should there be a possibility of non-resonant frequencies being applied to the sonar transducer drive circuit.

Another feature of the PA04 which is especially helpful in battery operations is its sleep mode function which can be used to turn the amplifier off during periods of non-use to minimize battery drain. Sleep mode quiescent current is only 5mA and the output is turned off into a high impedance state.

One caution when using sleep mode is to be aware of transients up to the supply rail that can occur during transitions into and out of sleep mode. There is no esoteric way to eliminate these internal to the op amp. If these transients would provide undesired transmissions, the problem can be cured through the use of two Schottky diodes (D3,D4) and two MOSFET switches (Q3,Q4). These components short the output of the PA04 to ground during the sleep mode transitions.

Timing logic going into sleep mode is to first command the input to zero, switch on Q3 and Q4 and then enable sleep mode. Coming out of sleep mode we would first ensure input signal is zero, ensure Q3 and Q4 are on, disable sleep mode, turn off Q3 and Q4, and finally begin transmitting with our input signal. Typical delay time to squelch the sleep mode transients is about 5-10 mS.

As a final note, to minimize SOA stresses it is advised to always start the input signal at zero crossing and exponentially ramp the amplitude if possible, since a transformer really doesn't look like a transformer until we have passed a few cycles of AC through it.