CDB4220/1/2/3/4

Evaluation Board for CS4220/1/2/3/4

Features

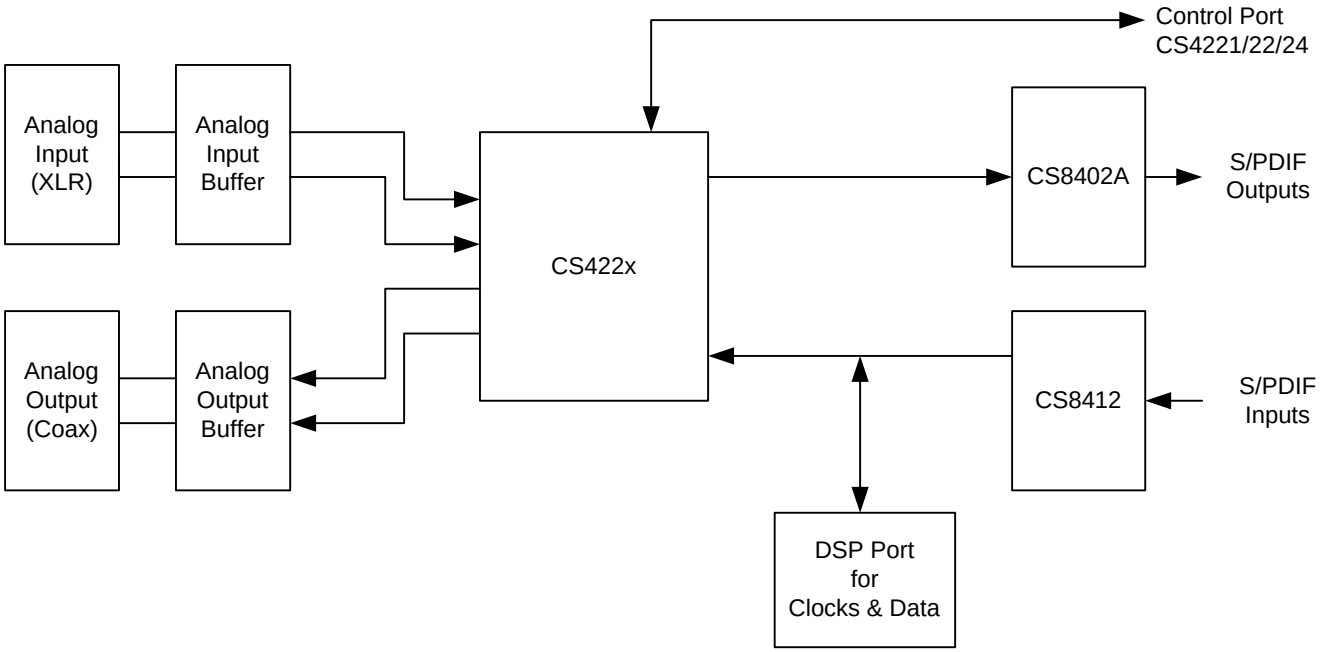
- Demonstrates recommended layout and grounding arrangements
- CS8412 receives AES/EBU, S/PDIF and EIAJ-340 compatible data
- CS8402A transmits AES/EBU, S/PDIF and EIAJ-340 compatible data
- Stereo Analog I/O
- DSP port for external serial audio I/O
- Windows 95® software interface to control CS4221/2/4
- Digital and Analog patch areas

General Description

The CDB4220 evaluation board is an excellent means for quickly evaluating the CS4220/1/2/3/4 family of stereo audio CODECS. Evaluation requires an analog signal source and analyzer, digital signal source and analyzer, PC compatible computer for device control and a power supply.

System timing can be provided by the CS8412 digital audio receiver, DSP Port or an on-board oscillator. Stereo analog input (XLR) and stereo analog output (coax) is provided. Digital I/O is provided through either the S/PDIF or DSP port. An SPI/I^2C serial control port allows the CS4221/2/4 to be configured and controlled using the supplied Windows 95® software.

ORDERING INFORMATION: CDB4220, CDB4221, CDB4222, CDB4223, CDB4224



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

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Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/

1. CDB4220 SYSTEM OVERVIEW

The CDB4220 evaluation board is an excellent means of quickly evaluating the CS4220/1/2/3/4 family of stereo audio codecs. Input and output analog interfaces are provided, and a CS8412 digital audio interface receiver and CS8402A digital audio interface transmitter provide an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board allows you to supply external clock and data signals through the 20-pin DSP port.

The CDB4220 schematic is partitioned into eleven schematics as shown in Figures 1 though 11.

2. CS4220/1/2/3/4 CODEC

A complete description of each member of the CS4220/1/2/3/4 family is included in each respective product datasheet.

3. CS8412 DIGITAL AUDIO RECEIVER

Performance of the DAC can be quickly tested by connecting a S/PDIF audio source to the CS8412. The S/PDIF signal may be input through either the optical or coax connector, see Figure 7. Please note that the two input connectors must not be driven simultaneously. The interface for the CS8412 includes a serial bit clock, serial data, left-right clock (FSYNC) and a 256 Fs master clock. The recovered MCLK, SCLK and LRCK provide the necessary clocks for the CS4220/1/2/3/4.

4. CS8402A DIGITAL AUDIO TRANSMITTER

Performance of the ADC can be quickly tested by connecting an analog generator to the left and right inputs and connecting the S/PDIF optical or coaxial output to audio test equipment. The evaluation board relies on the CS8412 or external clocking signals input through the DSP port for all clocking. The recovered clock from the CS8412 receiver has a frequency of 256 Fs. The CS8402A requires a master clock frequency of 128 Fs, and the 74HC74 divides the MCLK by 2 to generate the proper clock signal.

5. ANALOG INPUT BUFFER

The analog inputs of the CDB4220/1/2/3/4 use dual op-amps to implement the AC coupled input buffer. This buffer also performs DC level shifting; a resistive divider supplies an approximate 2.3V bias voltage to the op-amps to set the input bias to the converter inputs. The inputs are digitally filtered after conversion to eliminate any offset. A nominal 5.66 Vpp drive to the buffer will apply a 2V rms differential input to the CS4220/1/2/3/4 resulting in a full-scale output.

6. ANALOG OUTPUT BUFFER

Each DAC output drives an op-amp that is configured as a differential to single-ended converter. This circuit also performs two-pole Butterworth filtering and is AC coupled to the output jack. Note that the signal paths through the evaluation board are non-inverting.

7. DSP PORT

The DSP HEADER (J5) port provides an interface to the serial audio clocks and data of the CS4220/1/2/3/4 and may be used to interface to external digital signal processors for ease in evaluating complete digital audio system solutions. Please note that when the DSP HEADER port is enabled, care should be exercised in using these signals because these lines require the proper buffers to enabled. By setting the DSP mode byte through the control port (CS4221/2/4) or setting the appropriate jumpers (CS4220/3), the data format can be modified to accommodate different DSP processors.

8. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board through four binding posts (-12V, +12V, AGND, +5VA) as shown in Figure 6. The +5VA input provides the +5 Volt power to the CS4220/1/2/3/4. Digital power is derived from the analog supply with a resistor and

additional decoupling capacitors. The ±12 V binding posts carry power to the analog input and output buffers. All power supply connections are bypassed with transient suppression diodes and bulk filtering capacitors.

9. CDB4221/2/4 CONTROL PORT SOFTWARE

The CDB4220 is shipped with Windows based software for interfacing with the CS4221/2/4 control port through the DB25 connector, J18. The software can be used to communicate with the CS4221/2/4 in either SPI or I^2C mode. Please note that the control port registers are write-only when SPI mode is used.

Run SETUP.EXE from the distribution diskette to install the software. Further documentation for the software is available on the distribution diskette in the plain text format file, README.TXT.

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J6	Select DSP port as slave	DISABLE DSP SLAVE	Configures DSP Port for slave mode operation*
J7	Select DSP port as master	DISABLE DSP MASTER	Configures DSP Port for master mode operation*
J8	Enable DSP port, enabling serial data I/O	DISABLE DSP ENABLE	Enables DSP Port operation* Disables DSP Port operation*
J9	Selects CS422x MCLK source	8412 DSP	CS422x MCLK supplied from CS8412 CS422x MCLK supplied from DSP Port
J10	Selects Loopback or Normal routing of data	1 0	Loopback - Routes SDOUT from A/D to SDIN of D/A Normal Operation
J11	Selects which codec is on the evaluation board	1 0	CS4220/1/3/4 CS4222
J12	DEM0	1 0	See CS422x datasheet for details
J13	DIF0(SDA/CDIN)	1 0	See CS422x datasheet for details
J14	DIF1	1 0	See CS422x datasheet for details
J15	CS422x Master/Slave Select	1 0	CS422x is configured for slave mode operation CS422x is configured for master mode operation
J16	$\overline{\text{SMUTE}}$ (CS4222 only)	1 0	Disables Soft Mute function of CS4222 Enables Soft Mute function of CS4222
J17	DEM1	1 0	See CS422x datasheet for details
J19	Selects which codec is on the evaluation board	4220/3 4221/2/4	CS4220/3 CS4221/2/4
J24	CS8412 Master/Slave Select	S M	CS8412 is configured for slave mode operation CS8412 is configured for master mode operation
J25	RCV PWR	OPEN CONNECT	Disables +5V power to CS8412 Supplies +5V power to CS8412
J26	CS8412 SDATA Routing	OPEN CONNECT	Routes SDATA to SDIN of CS422x
J27	CS8412 SCK Routing	OPEN CONNECT	Routes SCK to SCLK of CS422x
J29	CS8412 FSYNC Routing	OPEN CONNECT	Routes FSYNC to LRCK of CS422x
J31	CS422x SDOUT Routing	OPEN CONNECT	Routes SDOUT to SDATA of CS8402A

Table 1. CDB4220-4 Jumper Selectable Options

* DSP Port jumper labels on evaluation board are backwards. Please see schematic for clarification.

	PURPOSE	CS4220	CS4221	CS4222	CS4223	CS4224
J6	Select DSP port as slave*	SLAVE	SLAVE	SLAVE	SLAVE	SLAVE
J7	Select DSP port as master*	MASTER	MASTER	MASTER	MASTER	MASTER
J8	Enable DSP port, enabling serial data I/O*	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
J9	Selects CS422x MCLK source	8412	8412	8412	8412	8412
J10	Selects Loopback/Normal routing of data	1	1	1	1	1
J11	Selects which codec is on the evaluation board	1	1	0	1	1
J12	DEM0	1	OPEN	1	1	OPEN
J13	DIF0(SDA/CDIN)	0	1	1	0	1
J14	DIF1	0	OPEN	OPEN	0	OPEN
J15	CS422x Master/Slave Select	1	1	1	1	1
J16	$\overline{\text{SMUTE}}$ (CS4222 only)	OPEN	OPEN	1	OPEN	OPEN
J17	DEM1	1	OPEN	1	1	OPEN
J19	Selects which codec is on the evaluation board	1	0	0	1	0
J24	CS8412 Master/Slave Select	M	M	M	M	M
J25	RCV PWR	CONNECT	CONNECT	CONNECT	CONNECT	CONNECT
J26	CS8412 SDATA Routing	OPEN	OPEN	OPEN	OPEN	OPEN
J27	CS8412 SCK Routing	CONNECT	CONNECT	CONNECT	CONNECT	CONNECT
J29	CS8412 FSYNC Routing	CONNECT	CONNECT	CONNECT	CONNECT	CONNECT
J31	CS422x SDOUT Routing	CONNECT	CONNECT	CONNECT	CONNECT	CONNECT

Table 2. CDB4220-4 Default Jumper Settings

* DSP Port jumper labels on evaluation board are backwards. Please see schematic for clarification.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5VA	Input	+5 Volt Power
AGND	Input	Analog Ground connection from power supply
+12V	Input	+12 Volt Power for op-amps
-12V	Input	-12 Volt Power for op-amps
LEFT	Input	Left channel analog input through XLR connector
RIGHT	Input	Right channel analog input through XLR connector
ANALOG OUT LEFT	Output	Left channel analog output through coaxial connector
ANALOG OUT RIGHT	Output	Right channel analog output through coaxial connector
XMITTER	Output	Digital audio interface output through coaxial connector
XMITTER OPT2	Output	Digital audio interface output through optical connector
RCVR	Input	Digital audio interface input through coaxial connector
OPT1 RCVR	Input	Digital audio interface input through optical connector
J18	Input/Output	I/O for I^2C or SPI control port signals through DB25 connector
DSP HEADER	Input/Output	I/O for external serial audio data and clock signals

Table 3. System Connections

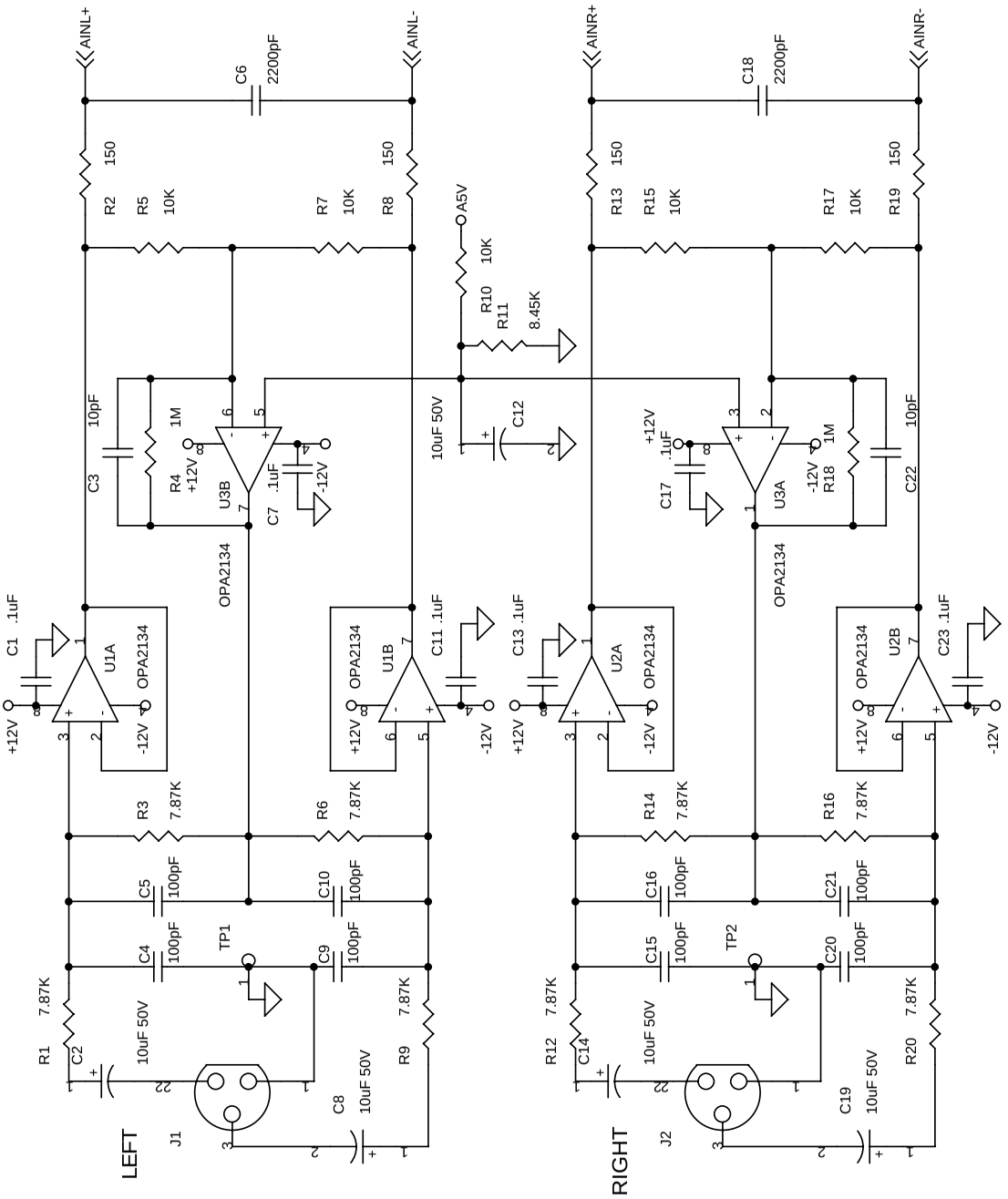

Figure 1. Analog In

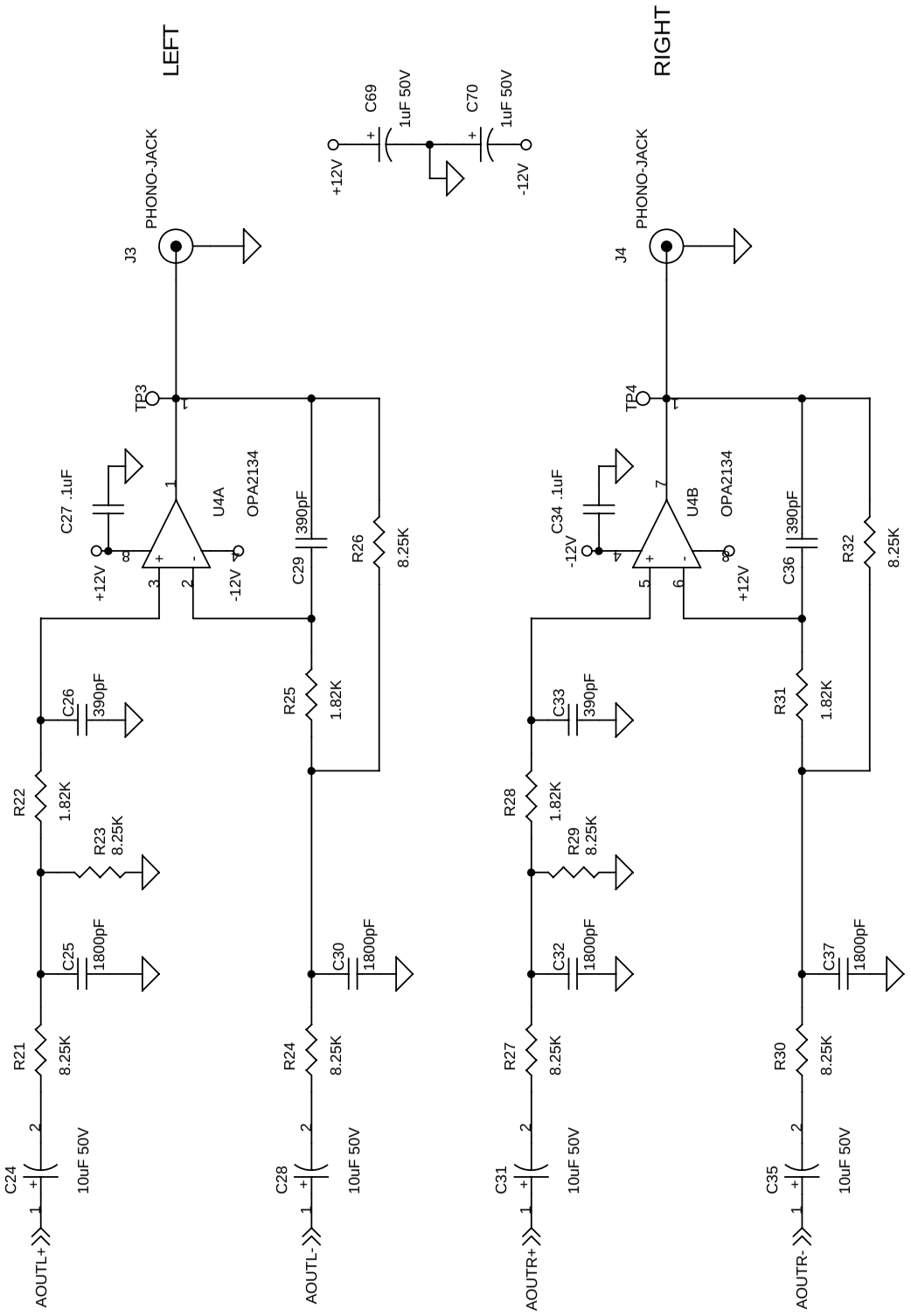

Figure 2. Analog Out

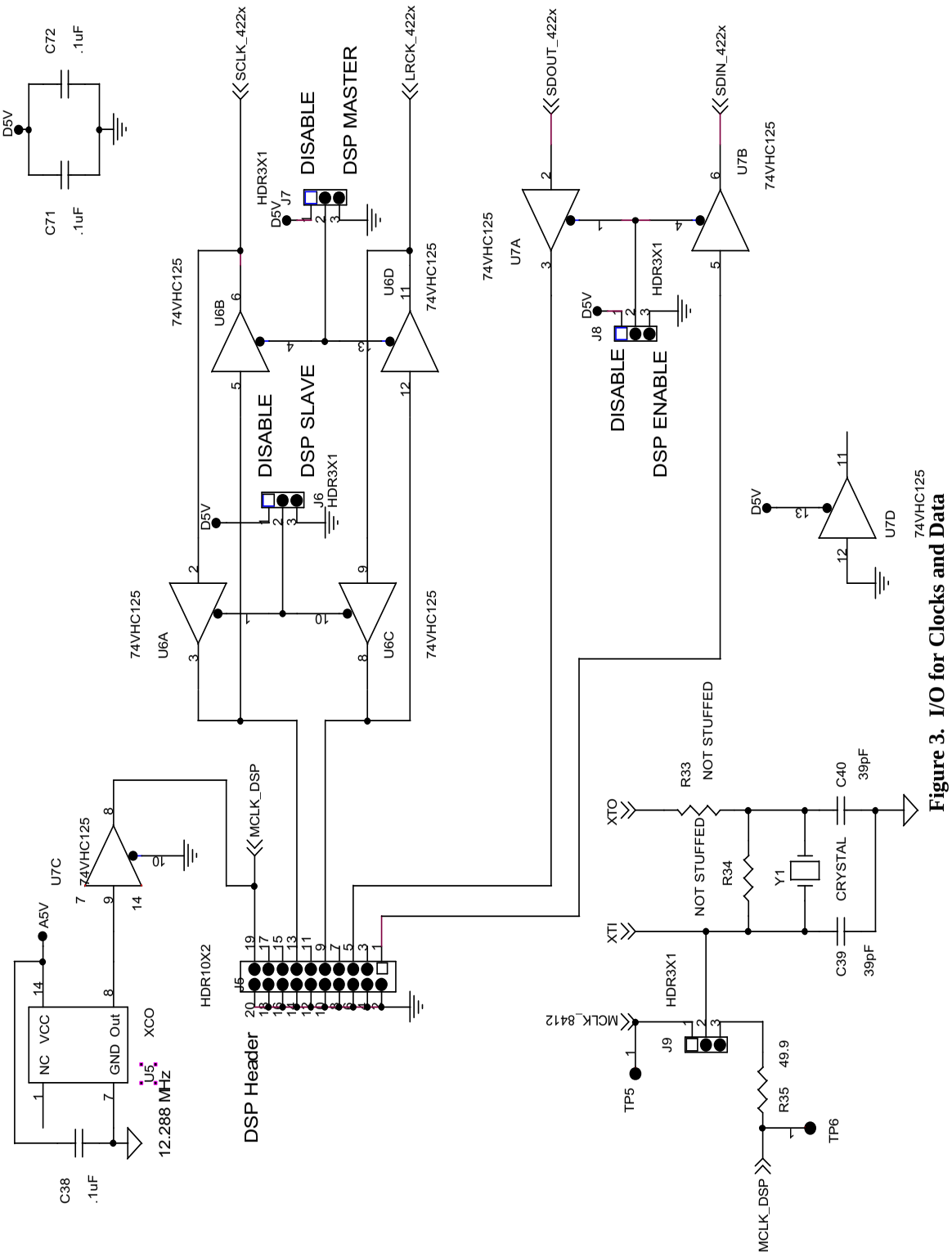

Figure 3. I/O for Clocks and Data

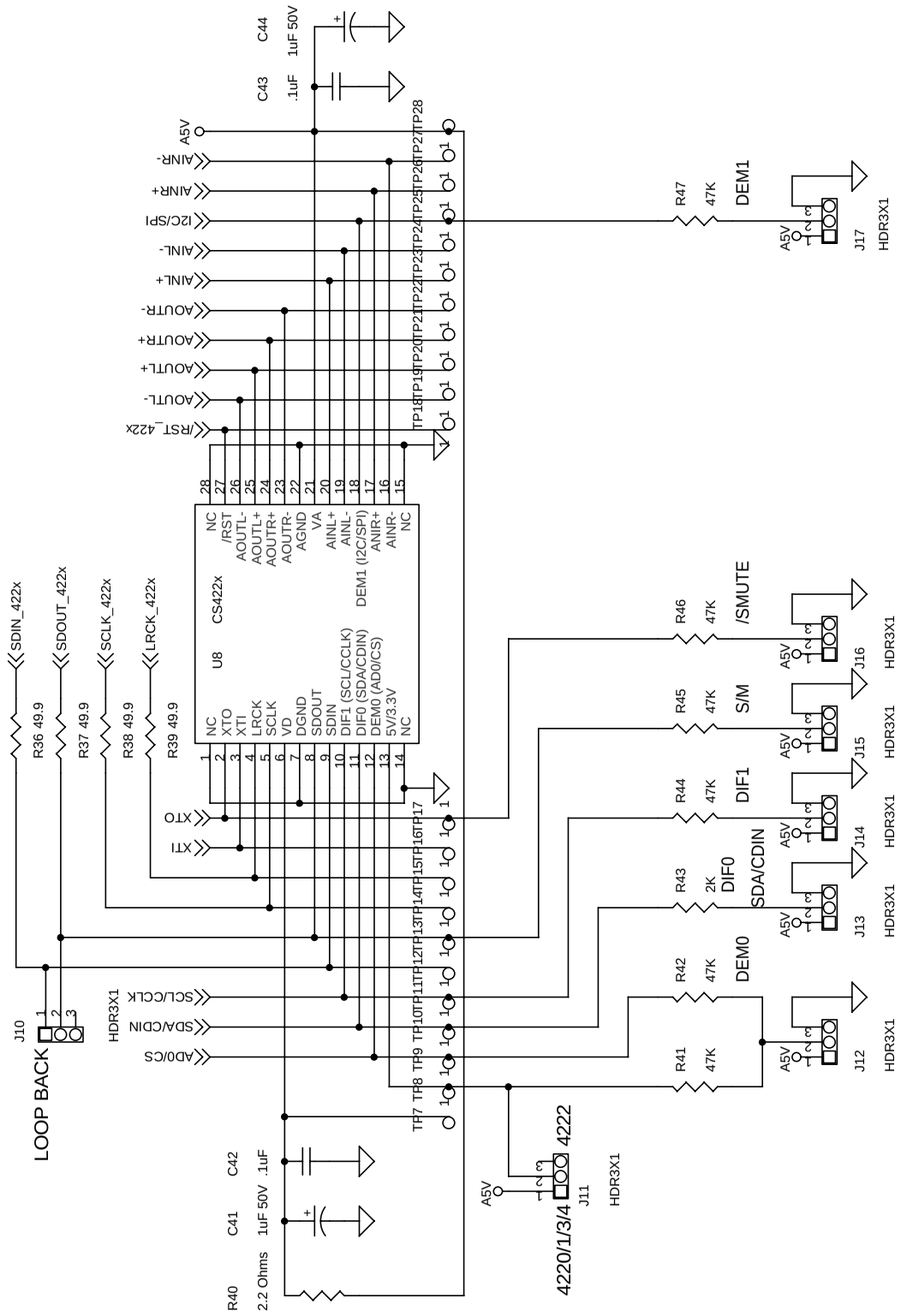

Figure 4. CS422x

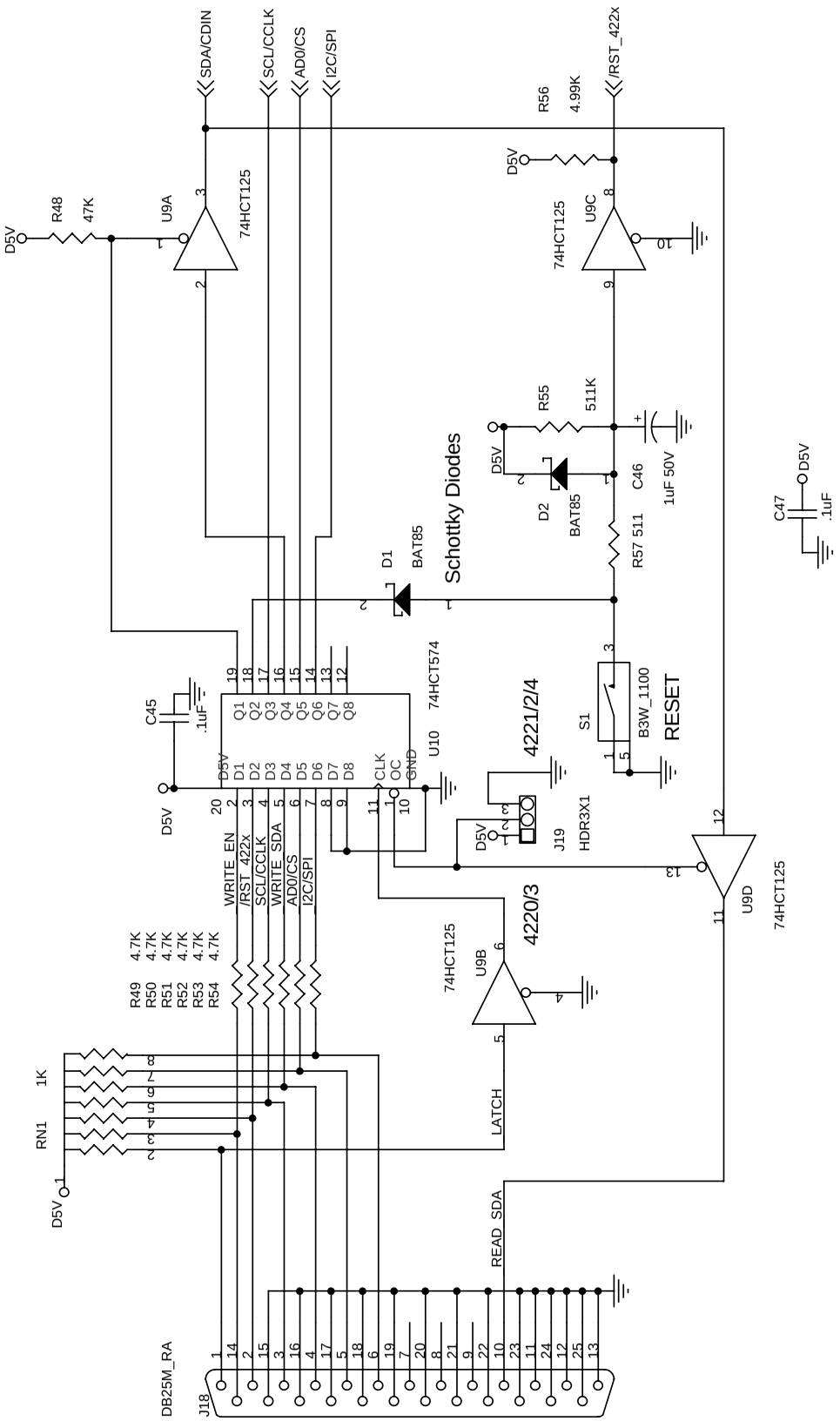

Figure 5. Control Port Interface

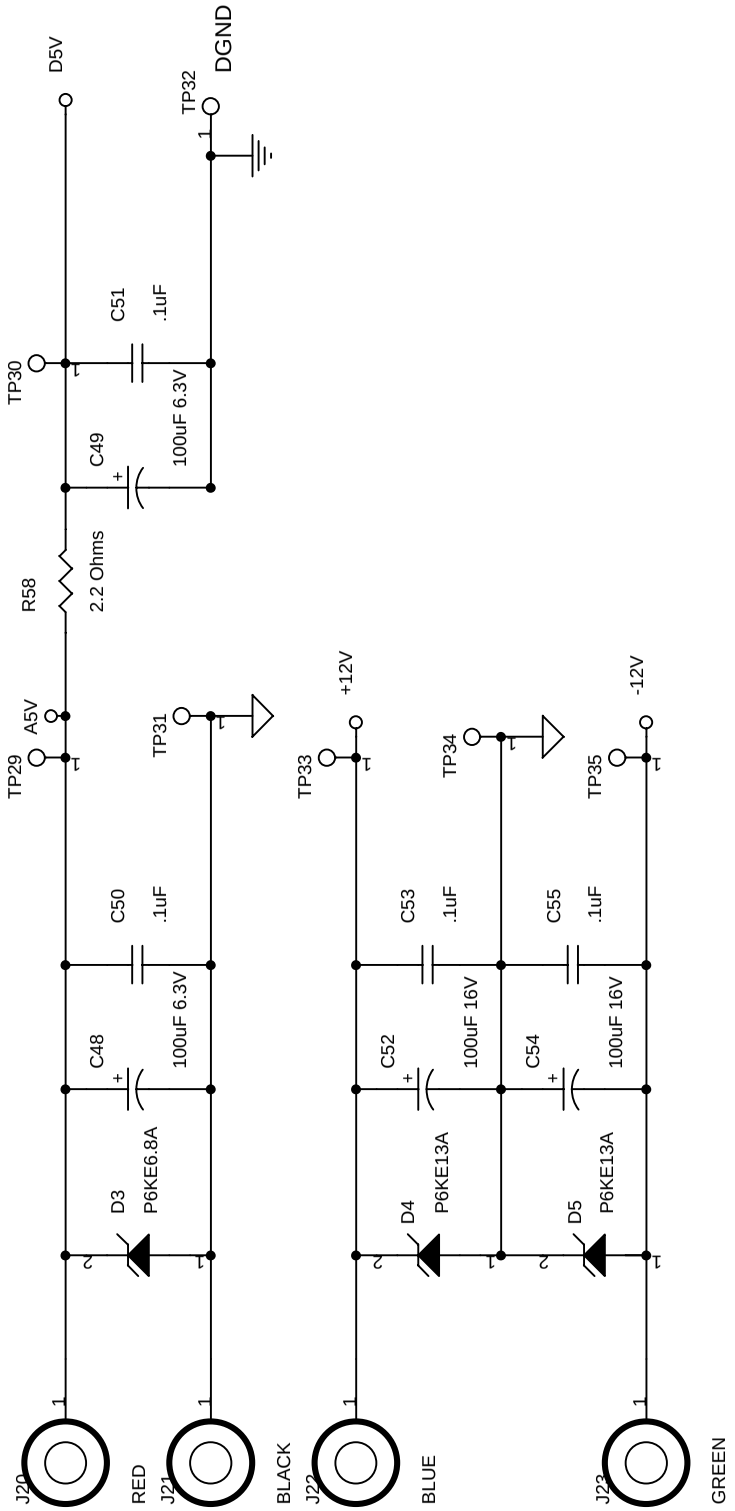

Figure 6. Power Supply

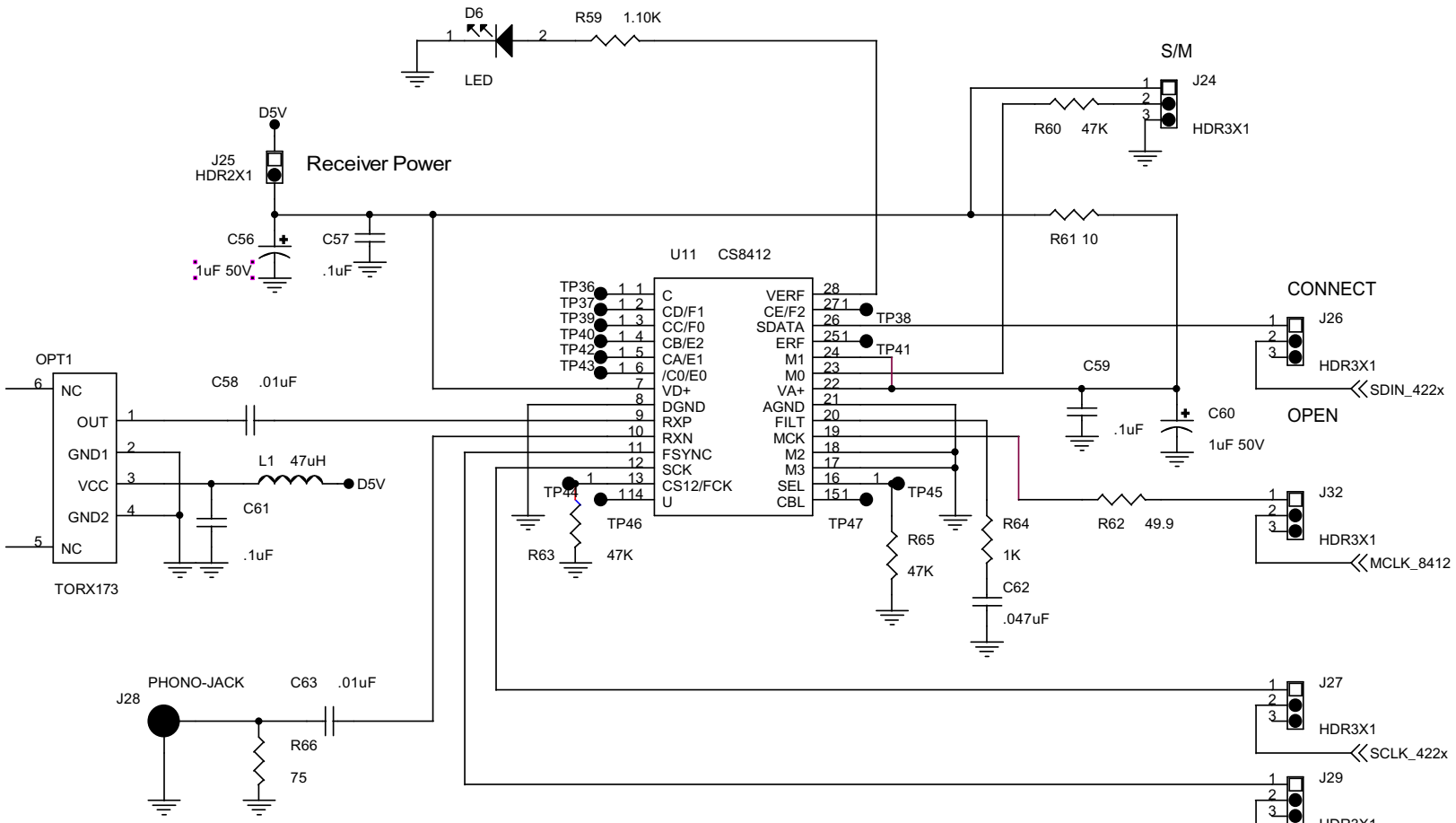

Figure 7. CS8412 Digital Audio Receiver

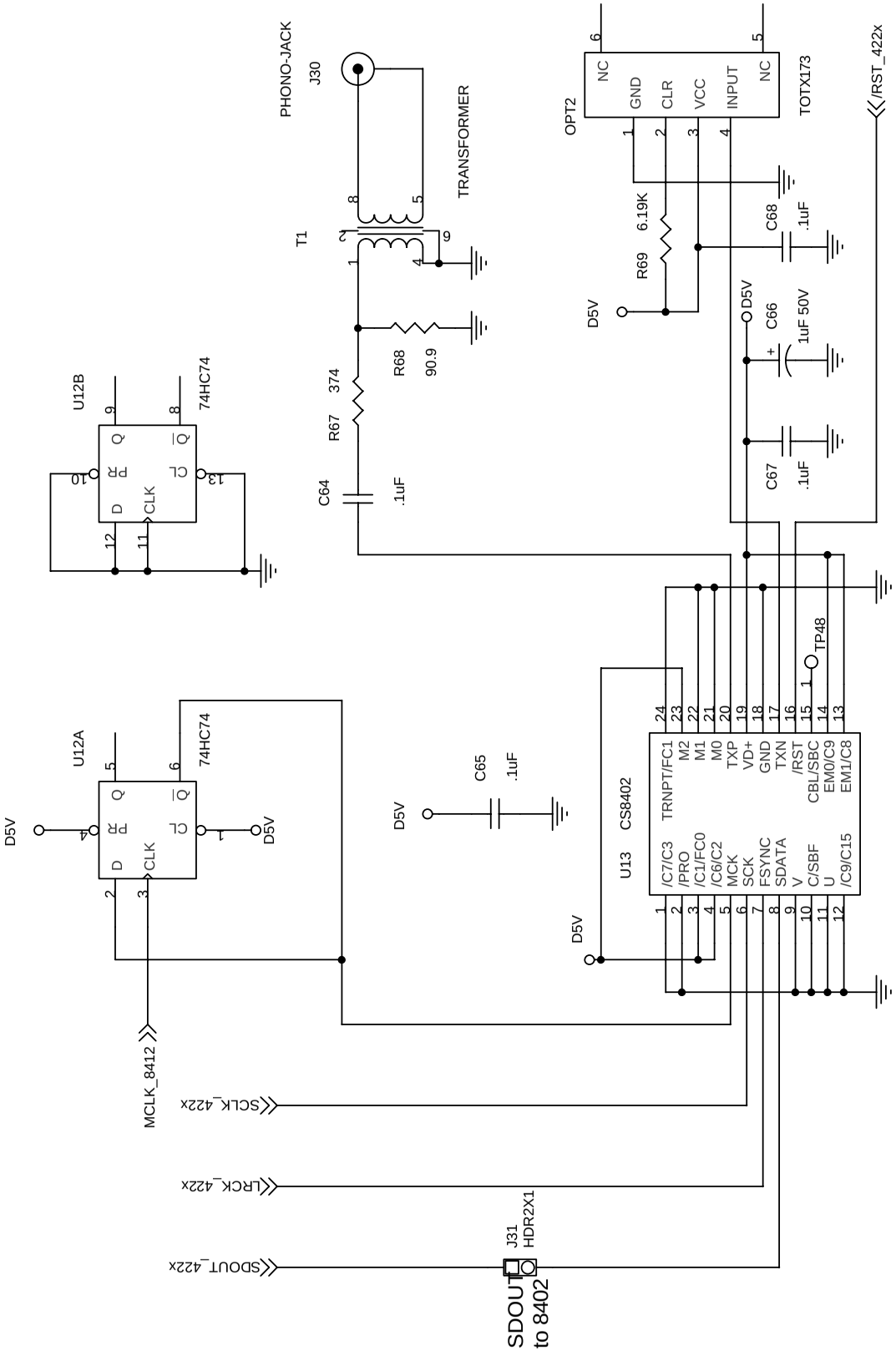

Figure 8. CS8402A Digital Audio Transmitter

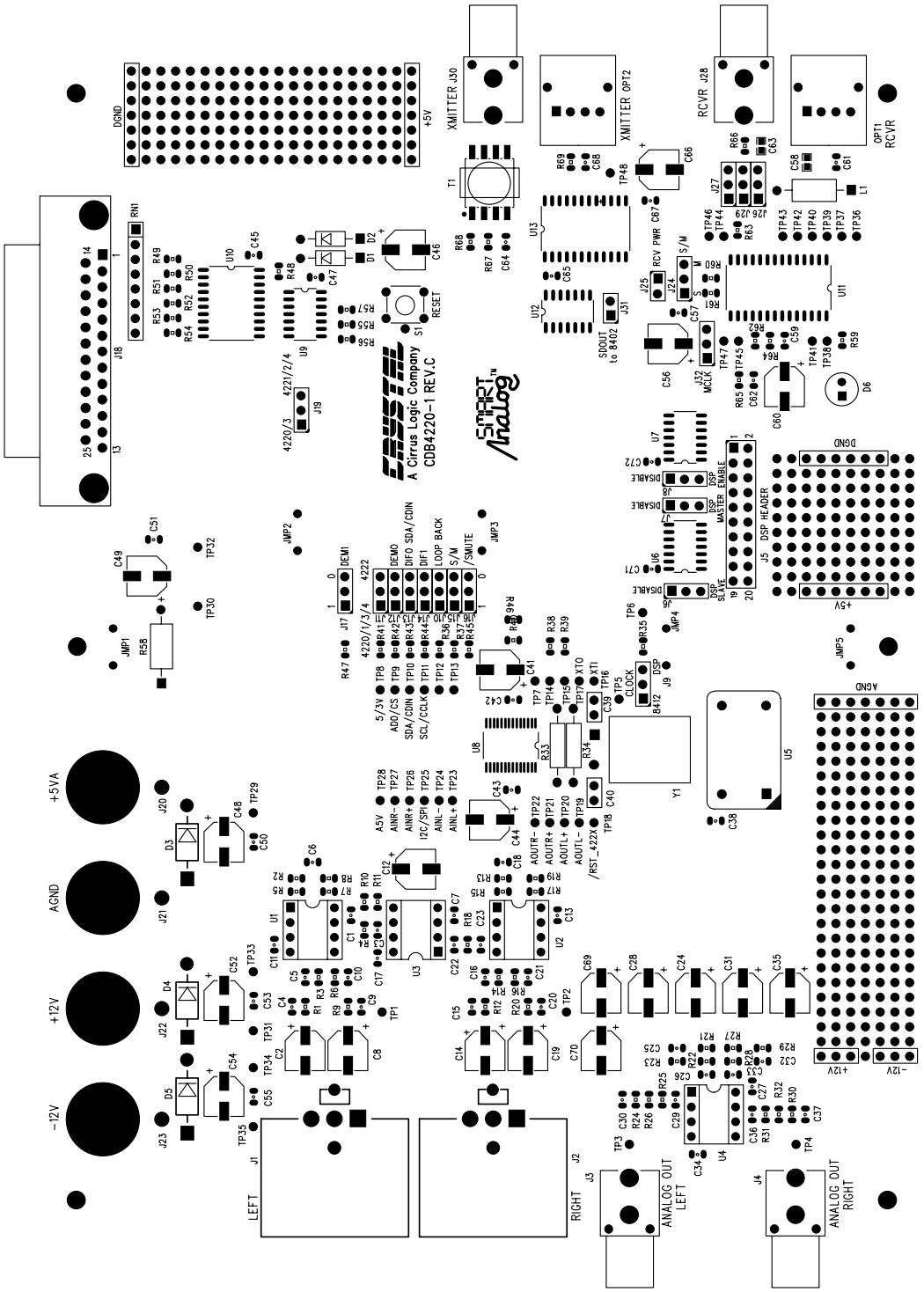

Figure 9. Top

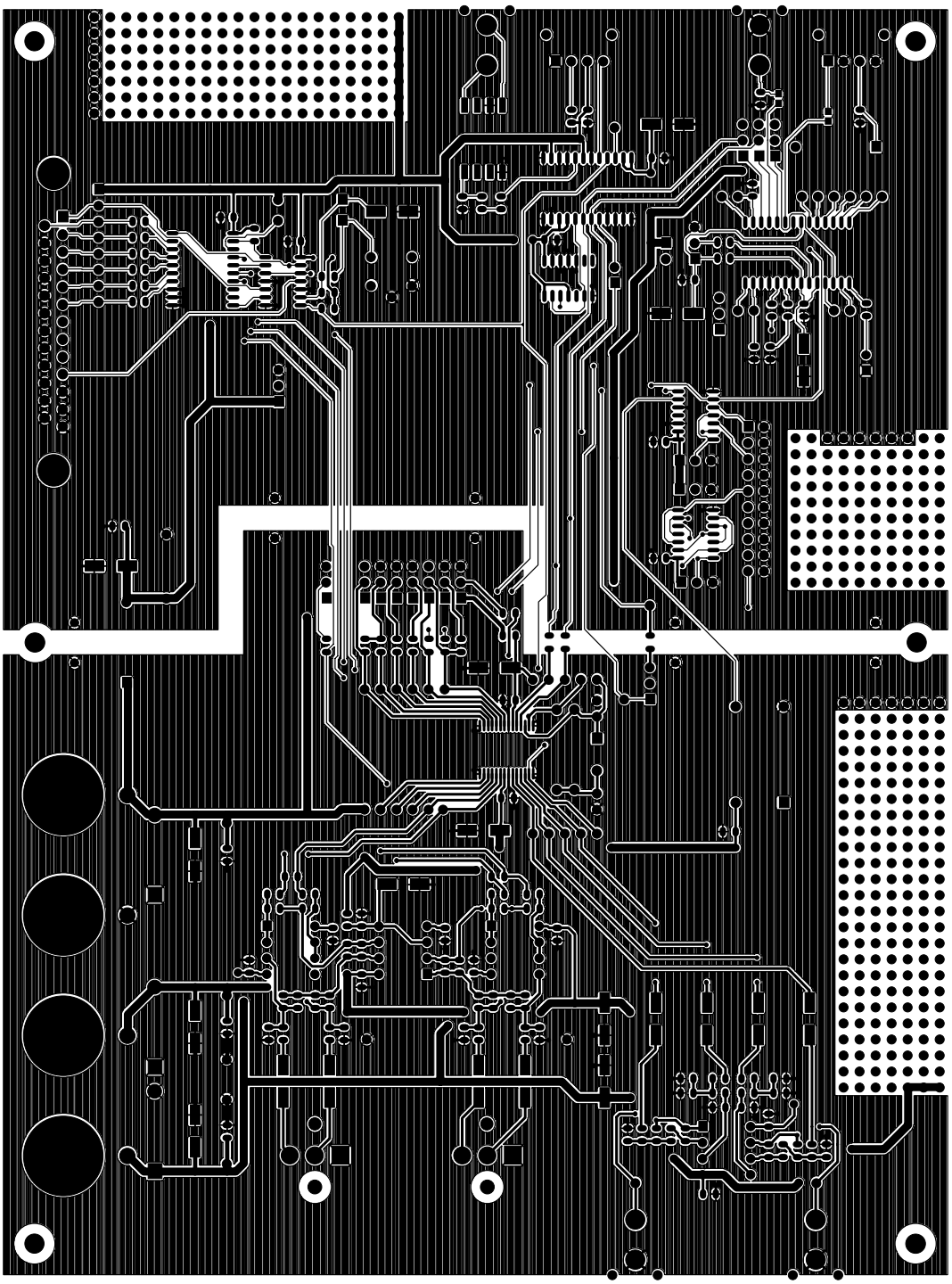

Figure 10. Top Silkscreen

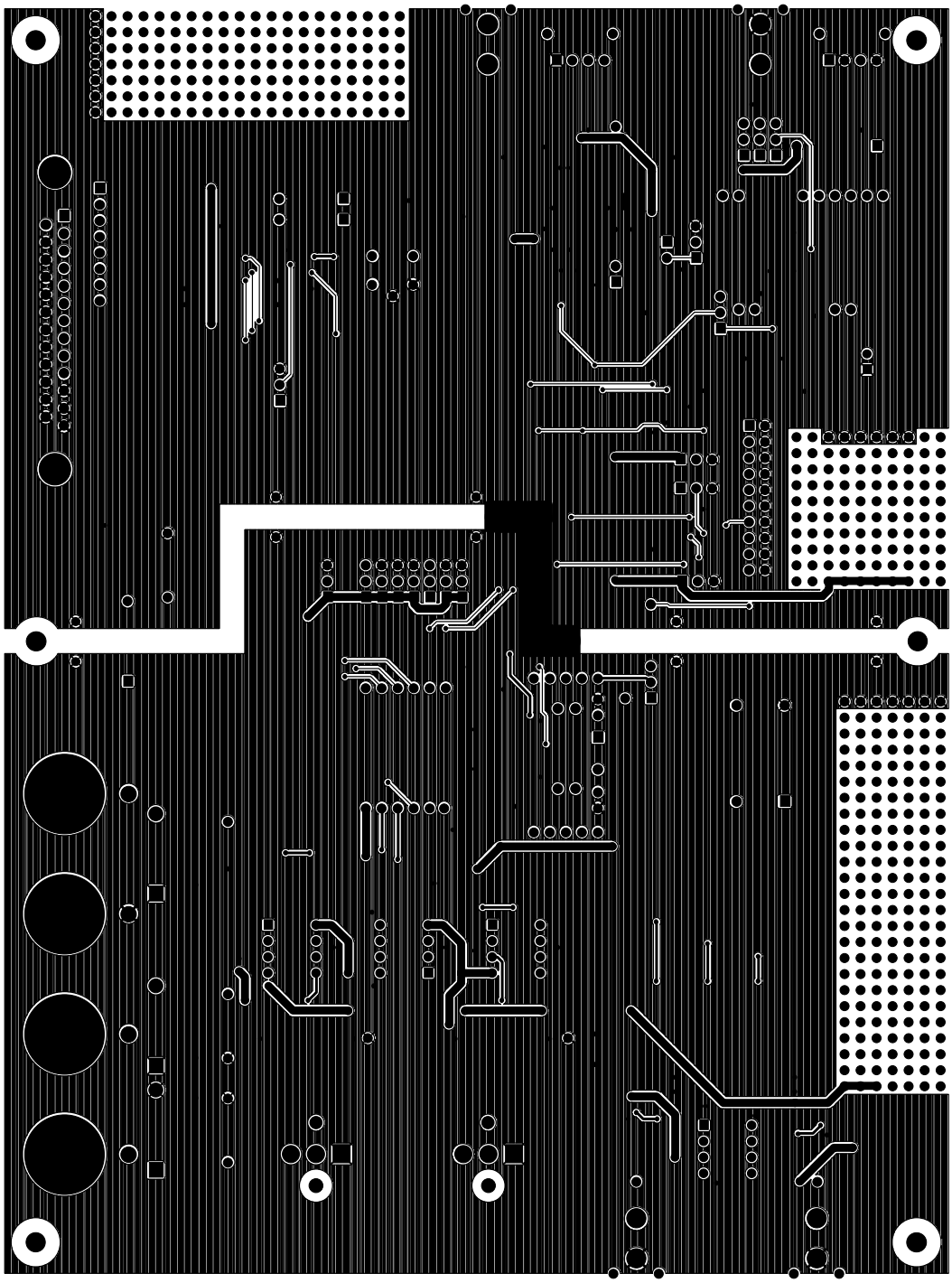

Figure 11. Bottom Silkscreen


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