# Technical Bulletin: CS1501 and CS1601 Overpower Protection in the CS1501/CS1601

## 1. Introduction

The CS1501 and CS1601 are high-performance Variable Frequency Discontinuous Mode (VF-DCM), active digital power factor correction (PFC) controllers designed with internal overpower protection (OPP). This note will describe the function of the protection circuit.

## 2. Description

Most PFC controllers are designed with current sensing to provide protection during an overpower (overcurrent) event. The CS1501/CS1601 uses its control algorithm to limit power as a function of the inductor current. Upon detection of a large, sustained overload, the IC shuts down for ~2 seconds, then restarts.

The fundamental action of an inductor requires the volts-seconds to be zero.

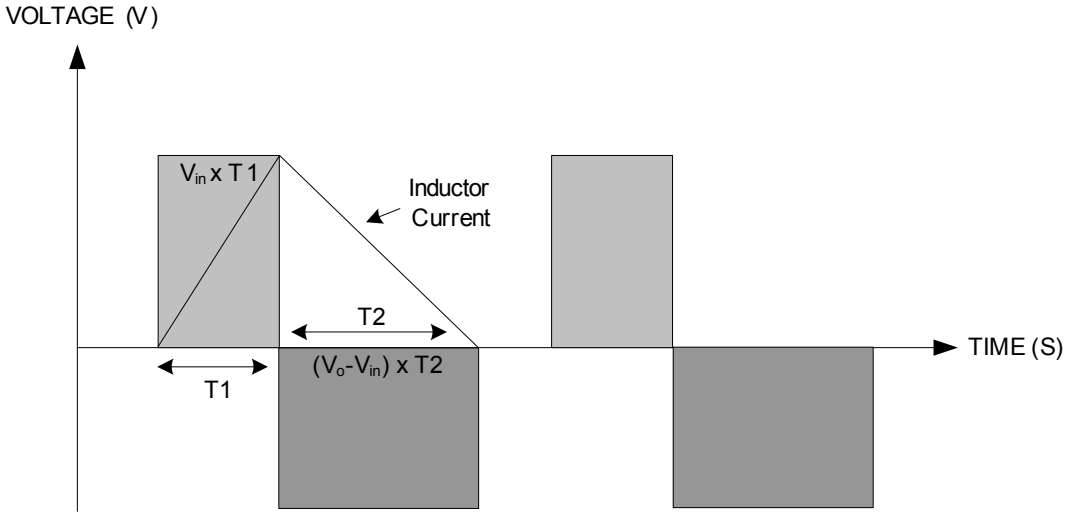


**Figure 1. Volts-Seconds Balance for a DCM Inductor**

The control algorithm of the CS1501/CS1601 guarantees VxT = 0 across the inductor for each switching cycle.

The basic equation for an inductor is:

$$V = L\frac{dI}{dT} \qquad \text{[Eq. 1]}$$

Given Inductance (L), Input Voltage ($V_{in}$), Output Voltage ($V_{link}$), Period (T), and DCM, this yields one solution for the inductor's peak current, setting the maximum load current ($I_{max}$).

When $I_{max}$ is reached:

- $V_{link}$ starts to droop.
- The PFC controller's voltage control loop has gone to its maximum.
- The circuit maintains PFC, operating in transition mode.

Under moderate overload, $V_{link}$ may droop up to 10% while maintaining rated power and PFC. Further increasing the load current causes $V_{link}$ to drop below the startup threshold (~90% of $V_{link}$). Below this threshold, the circuit changes its operating mode to startup, and more power is available to raise $V_{link}$. As $V_{link}$ reaches its nominal value, startup mode is canceled and power is now limited to the rated value. For a fuller description of startup, see below.

- Repeated overload causes $V_{link}$ to droop again, and the cycle is restarted.
- There is a narrow range of overload between system-rated power and startup power where the modes alternate, averaging to the required power.
- High overloads keep the system permanently in startup mode, never reaching $V_{link}$.
- Extreme overloads disable the PFC operation, resulting in $V_{link}$ being peak rectified.

## 3. Various Overload Conditions and System Response

- A short or low-resistance path across the link capacitor will blow the fuse.
- Less severe overloads can be handled permanently or temporarily.
- A momentary overload on a secondary converter may propagate to the PFC stage. This is seen as a transient on $V_{link}$ and will stabilize quickly.
- The device is designed to ride over occasional load surges before shutting down.
- When the device detects a sustained overload or a repeated cycle of overload events, it stops PFC action.

## 4. Action of IC During startup

- The startup algorithm is designed to deal with $V_{link}$ being as low as one diode drop below $V_{in}$ (AC peak).
- The algorithm delivers more than the rated power (>125%) but does not guarantee PFC.
- During startup, the inductor's peak current may exceed the normal operating current at full load, $V_{in}$ (AC) minimum.

## 5. Overcurrent (Current Sense) Protection.

Under some extreme operation conditions, such as rapid load transitions or high-speed transients on the AC line, the digital algorithm may not be able to adequately control the peak current in the Boost MOSFET. To safeguard against these conditions, overcurrent protection (OCP) is used.

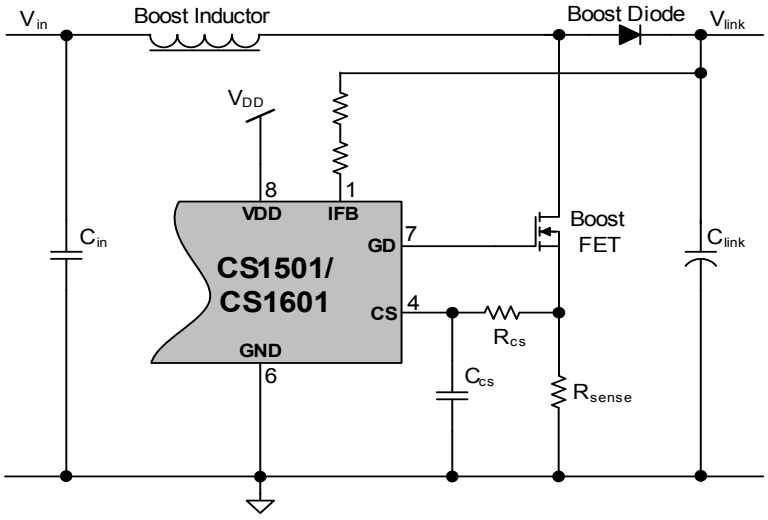


**Figure 2. CS1501/CS1601 Current Sense**

OCP is accomplished by placing a resistor, $R_{sense}$, in series with the Boost FET source (Figure 2.) The current is sensed as a voltage across $R_{sense}$. This is connected to the current sense pin of the IC (pin 4 CS). When the voltage exceeds an internal reference value, the gate driver GD (pin 7) is forced low (ground), turning off the FET.

The internal circuit monitors the current sense input and provides two error outputs. These are:

1) CS_MID: Cycle-by-cycle current sense monitoring with current threshold set slightly above $I_{peak}$.

2) CS_HIGH: A catastrophic overcurrent event monitoring block with current threshold set to 2 times $I_{peak}$

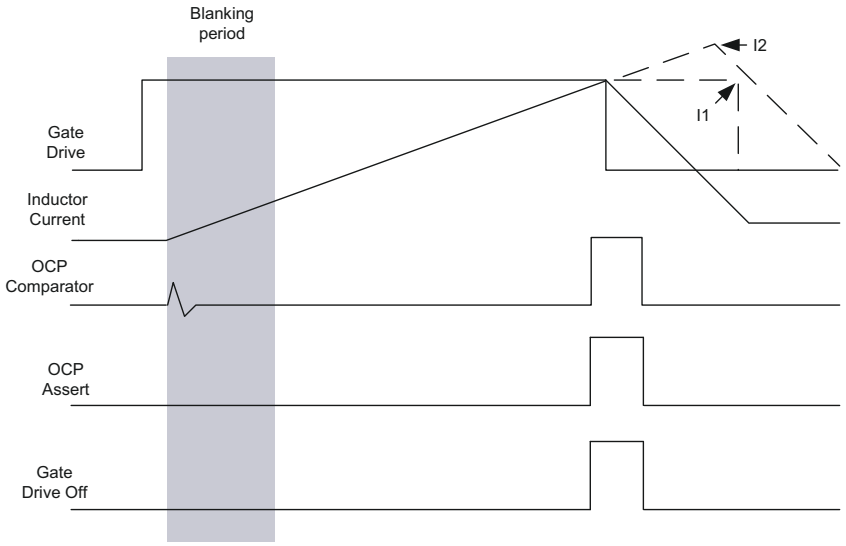


**Figure 3. Overcurrent Thresholds and Timing**

## 6. Operation of Internal OCP Functions

The internal control algorithm determines the on-time of the FET, T1, depending on input and output voltage.

**CS_MID**

Cycle-by-cycle OCP limits inductor current through the FET, protecting it from damage due to high currents. At the gate drive edge, the sense output is ignored by activating blanking for 300nS to prevent false triggers. When the FET is turned on, the inductor current rises. If the current crosses the OCP threshold, I1, after the blanking period is completed, the logic triggers OCP Assert, forcing the gate drive to turn off before the calculated T1 is completed. I2 is the current that the inductor would use to internally calculate T1.

**CS_HIGH**

Similar to Mid-Threshold, CS_HIGH produces an OCP signal sent to gate drive off, and a second output, OCP latch, sent to a timeout counter. This monitors sudden above-normal inductor current. The threshold used here to trigger the comparator is twice that of CS_MID. When a CS_HIGH event occurs, the IC stops switching, automatically restarting after its timeout period (~2mS). The maximum delay between sensing an OCP event and turning the FET off is approximately 500nS.

## 7. Summary

Overpower protection (OPP) is guaranteed by a combination of external design (inductor value) and internal algorithm control. In addition to the internal OPP, an external overcurrent protection (OCP) circuit using a sense resistor in the source of the MOSFET is used to protect the system. OCP (CS_MID) is most likely to trigger at low input voltages, where the peak current under normal operation is highest. OPP is most likely to trigger at high AC line voltages, where the peak current under normal operation is low. Catastrophic overcurrent protection (CS_HIGH) functions under all conditions. Depending on the circuit design and test conditions, one of these detection circuits will trigger on a system fault protecting the system from abnormal currents and their associated risks to normal circuit operation.

## 8. Revision History

| Revision | Date | Changes |
|---|---|---|
| TB1 | JUN 2011 | Initial Release |

## Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to http://www.cirrus.com