

Errata: CS5342 Datasheet Errata

Rev E Silicon, Reference Datasheet DS608PP2

- CS5342 performance is not guaranteed for all extended sample rates as listed in the datasheet. Table 1 lists the acceptable ranges of Fs for each of the three speed modes.

Speed Mode	MCLK/LRCK Ratio	Output Sample Rate Range (kHz)
Single Speed Mode	768x	43-51
	384x	2-51
Double Speed Mode	384x	86-102
	192x	50-102
Quad Speed Mode	192x	172-200
	96x*	100-200

* Quad Speed Mode, 96x only available in Master Mode

Table 1. Speed Modes and the Associated Output Sample Rates (Fs)

- Page 10 of datasheet DS608P1 lists Switching Characteristics for the CS5342 Serial Audio Port. The restriction on extended sample rates as listed above implies an increase in the minimum SCLK period in Slave Mode as listed on page 10 of the datasheet. Table 2 lists the minimum SCLK period for each of the three speed modes.

Speed Mode	SCLK/LRCK Ratio	Minimum SCLK Period (ns)
Single Speed Mode	48x, 64x	408, 306
Double Speed Mode	48x	204
Quad Speed Mode	48x	104

Table 2. Minimum SCLK Period Requirements in Slave Mode