12/22/04

Errata: CS42528 Rev. C

(Reference CS42528 Data Sheet DS586PP5)

*All references to the CS42528 mentioned below shall be taken to refer to revision C of the CS42528 product. The hardware revision code can be found in the 12-character field printed on the last line below the part number of each chip. The letter that appears as the eighth character from the right is the revision code (e.g. YFTA**C**XAL0311 is a Revision C part).*

- S/PDIF receiver and PLL to SAI_LRCK operation is limited to sample rates from 32 kHz to 96 kHz.
- Upon disabling the PDN bit, the ADC will startup in one of two modes that affect dynamic range. In one mode the ADC's dynamic range will meet data sheet specification while in the other, the ADC's dynamic range will exhibit a degradation by approximately 4 dB. Which mode the ADC will enter upon the release of PDN is indeterminate.
- The PLL may either take a long time to lock to certain sample rates, or may not lock to them at all. The specific sample rates to which the a particular device has difficulty locking may vary depending upon many different parameters such as board layout, power supply level and noise, loop filter components, OMCK frequency, etc...

  The following work-around, including both steps 1 and 2, must be implemented to ensure that the PLL will lock to all sample rates:

  1. The PLL loop filter components must be as follows:
  - Rfilt = 2.55 kΩ
  - Cfilt = 0.047 µF
  - Crip = 2200 pF

  2. A series of control-port reads and writes must be executed in accordance with the flowcharts shown on the attached pages. Figure 1 on page 2 applies to applications that use one or both of the serial ports in master mode. Figure 2 on page 3 applies to applications that use both of the serial ports in slave mode. In slave mode only applications, the RMCK pin should be terminated with a 47 kΩ resistor to GND such that its state is determinate when the HiZ_RMCK bit is set.
- Register 02h bit 7 is reserved and must always be set to '0'.
- Register 24h bit 6 is reserved and must always be set to '0'.
- When reading from or writing to the control port, the memory address pointer (MAP) will always automatically increment regardless of the setting of the INCR bit (the MSB of the 8-bit MAP).

CONTACTING CIRRUS LOGIC SUPPORT

For a complete listing of direct Distributor, Sales, and Sales Representative contacts, visit the Cirrus Logic web site at www.cirrus.com

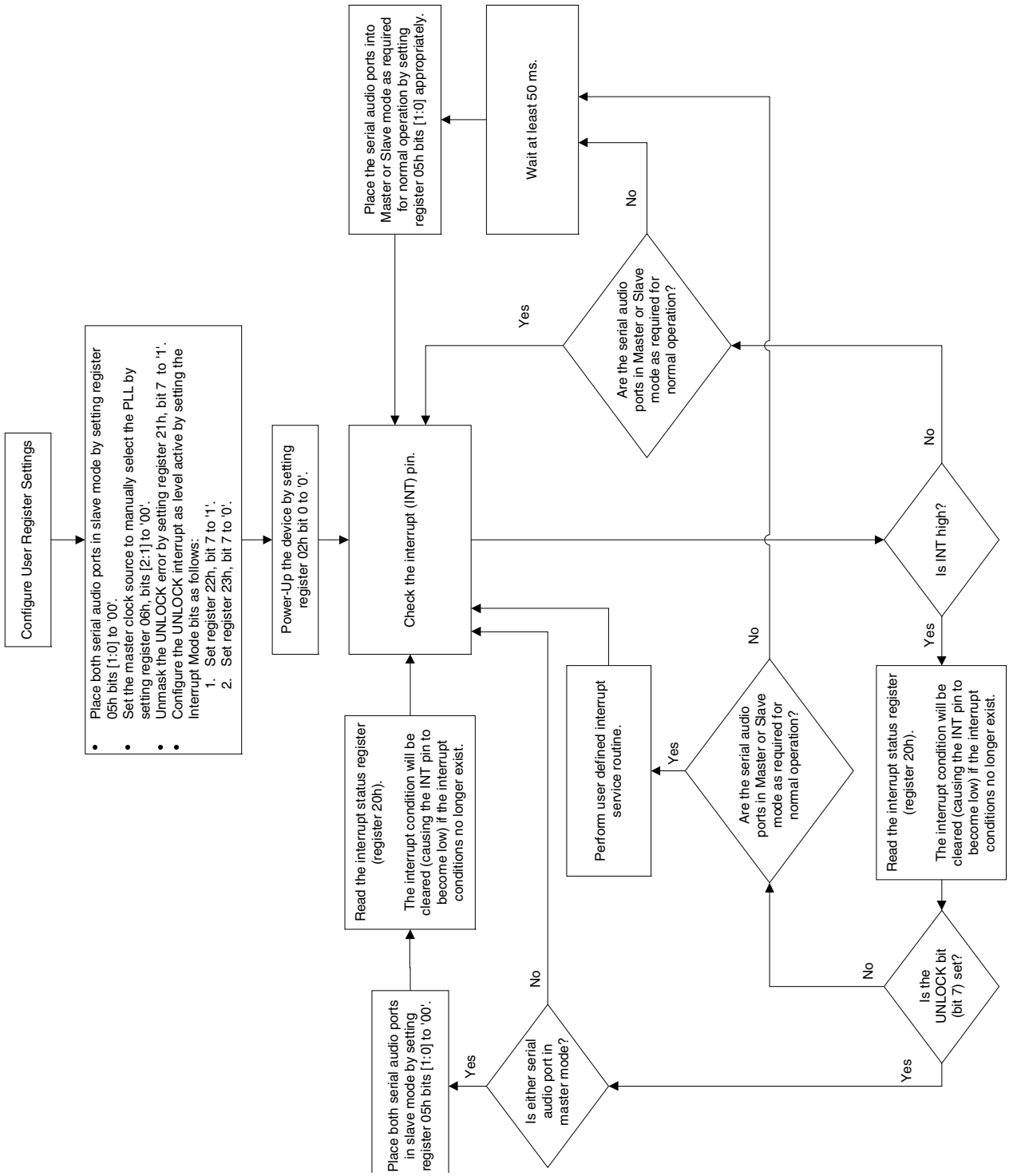

Figure 1. Master Mode Flowchart

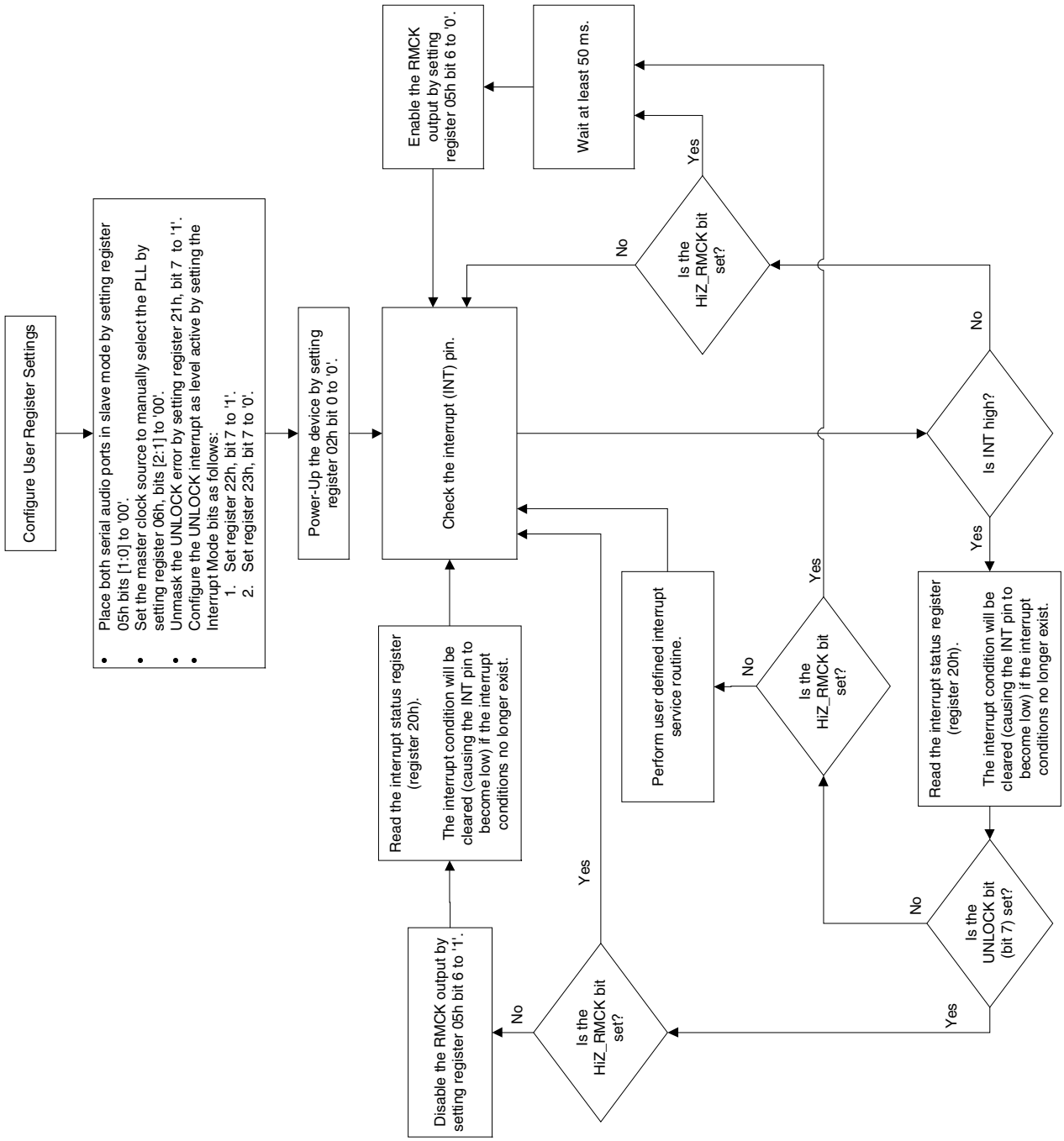

Figure 2. Slave Mode Only Flowchart