10/15/03

Errata: CS42528 Rev. B

(Reference CS42528 Data Sheet)

*All references to the CS42528 mentioned below shall be taken to refer to revision B of the CS42528 product. The hardware revision code can be found in the 12-character field printed on the last line below the part number of each chip. The letter that appears as the eighth character from the right is the revision code (e.g. YFTAD**B**XAL0311 is a Revision B part).*

- The Format Auto-Detection feature in the S/PDIF Receiver is not available.
- The General Purpose Outputs will not identify ADC Overflow conditions and cannot be set to Open Drain.
- The following register bits are not available:
  - Reg 05h[6] **RMCK HIGH IMPEDANCE (HIZ_RMCK)**
  - Reg 06h[0] **FORCE PLL LOCK (FRC_PLL_LK)**
  - Reg 08h[6:4] **AES FORMAT DETECTION (AES FORMATX)**
  - Reg 09h-0Ch [7:0] **BURST PREAMBLE BITS (PCX & PDX)**
  - Reg 1Eh[7] **SERIAL PORT SYNCHRONIZATION (SP_SYNC)**
  - Reg 1Eh[5:4] **DE-EMPHASIS SELECT BITS (DE-EMPHX)**
- The AUX [3:0] status field of the Receiver Channel Status register at address 25h reports information for channel A when CHS=1 and channel B when CHS=0.
- The DAC De-emphasis Control bit, DAC_DEM, does not properly control the de-emphasis filter. The failure could be either no de-emphasis is applied to the incoming signal when configured to do so, or de-emphasis is applied to a sample rate other than 32, 44.1 or 48 kHz. To ensure proper operation, it is recommend to always set the DAC_DEM bit to a ‘1’b prior to exiting the Power Down state, PDN=’0’b, or prior to changing the functional mode of the Codec Serial Port to single speed mode (CODEC_FM (1:0) = ‘00’b). Following this action, if de-emphasis is not required, turn the DAC_DEM bit off, ‘0’b.
- The Receiver Auto De-emphasis Control bit, RCVR_DEM, does not properly control the de-emphasis filter. The failure could be either no de-emphasis is applied to the incoming signal when configured to do so, or de-emphasis is applied to a sample rate other than 32, 44.1 or 48 kHz. To ensure proper operation, it is recommend to always set the RCVR_DEM bit to a ‘1’b prior to exiting the Power Down state, PDN=’0’b, or prior to changing the functional mode of the Serial Audio Interface Port to single speed mode (SAI_FM (1:0) = ‘00’b). Following this action, if de-emphasis is not required, turn the RCVR_DEM bit off, ‘0’b.

- The de-emphasis filter will incorrectly be applied to an incoming S/PDIF non-audio data stream if the channel status bits inappropriately indicate emphasis is applied and the RCVR_DEM bit in the Functional Mode control register at address 03h is enabled. The recommendation is to ensure the RCVR_DEM bit is turned off anytime the received data is non-audio.
- When the internal DAC and ADC are configured to use the recovered system clock from the S/PDIF interface, the THD+N performance will be degraded at higher input frequencies. As a result, audio frequencies above approximately 5 kHz will exhibit a decreased THD+N level of performance.

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