

WM8734 Evaluation Board User Handbook

INTRODUCTION

The WM8734 is a portable audio CODEC with headphone driver and programmable sample rates.

This evaluation platform and documentation should be used in conjunction with the latest version of the WM8734 datasheet. The datasheet gives device functionality information as well as timing and data format requirements.

This evaluation platform has been designed to allow the user ease of use and give optimum performance in device measurement as well as providing the user with the ability to listen to the excellent audio quality offered by the WM8734.

GETTING STARTED

PACKING LIST

The WM8734 Evaluation Kit contains:

- 1 WM8734-EV2B Evaluation Board (marked as WM8731_EV2)
- 2 WM8734-EV2S 3.5" floppy disks containing control software
- This manual -1 WM8734-EV2M

CUSTOMER REQUIREMENTS

Minimum customer requirements are:

- D.C. Power supply of +5V
- D.C. Power supply of +2.7V to +3.6V
- PC and printer cable (for software control)

Minimum spec requirements are:

- Win95/98/NT/2000/XP
- 486 Processor
- Approximately 1.5Mb of free disk space

DAC Signal Path Requires:

- Digital coaxial or optical data source
- 1 set of active stereo speakers or headphones

ADC Signal Path Requires:

- Analogue coaxial or 3.5mm jack plug data source
- Digital coaxial or optical data receiving unit

POWER SUPPLIES

Using the power leads provided with this evaluation kit, supplies should be connected as described in Table 1.

REF-DES	SOCKET NAME	SUPPLY
J7	DCVDD	+2.7V to +3.6V
J2	+5V	+5V
J3	DBVDD	+2.7V to +3.6V
J4	AVDD	+2.7V to +3.6V
J1	GND	0V
J6	AGND	0V

Table 1 Power Supply Connections

The GND and AGND connections may be connected to a common GND on the supply with no reduction in performance.

Note:

1. As standard, designator L5 will be populated with a zero ohm link so that a separate supply is not required for DBVDD. If separate supplies are to be connected, L5 should be unpopulated and +2.7V to +3.6V should be connected to the DBVDD panel socket (J3).
2. Refer to WM8734 datasheet for limitations on individual supply voltages.

Important: Exceeding the recommended maximum voltage can damage EVB components. Under voltage may cause improper operation of some or all of the EVB components.

BOARD FUNCTIONALITY

When using the DAC, there are three options for inputting digital data into the WM8734 evaluation board. There is a coaxial input (J15) via a standard phono connector or an optical input (U1) via a standard optical receiver module. A direct digital input is also available via one side of a 2x8 pin header (H1).

The analogue outputs of the board are via phono connectors J25 (LOUT) and J21 (ROUT) as well as a 3.5mm jack socket J28 (HPHONE).

When using the ADC the analogue input signals are applied to the evaluation board via phono connectors J8 (LLINEIN) and J12 (RLINEIN).

There are three options for outputting digital data from the WM8734 evaluation board when the ADC is used. There is a coaxial output (J26) via a standard phono connector or an optical output (U6) via a standard optical transmitter module. The digital signals output from the WM8734 may also be accessed via one side of a 2x6 pin header (H2).

All WM8734 device pins are accessible for easy measurement via the 14 pin headers (J13 & J17) running up each side of the device.

The software control mode (i.e. SPI or 2-wire) is selectable via a 2-pin jumper connection (J11).

A level-shift IC (U3) is used to shift the fixed +5V digital input from the CS8427 (U5) down to the same level as DBVDD. A transistor level-shift arrangement (Q1, Q2 & Q3) is used to shift the software digital control lines from the PC (fixed +5V) to the same level as DBVDD.

BOARD INPUT

The input interface to this board is via two analogue signal input phono connectors J8 (LLINEIN) and J12 (RLINEIN). These signals are AC coupled before being input to the device. To allow a 2Vrms input signal to be input to the evaluation board without causing damage to the WM8734, a simple resistor divider puts a 7dB attenuation on the input signal ensuring that a signal no greater than 1Vrms reaches the WM8734.

When used in Slave Mode digital clock signals **must** be supplied to the WM8734. A digital (AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201) signal input **must** be applied to either the coaxial input (J15), or the optical input (U1), allowing the CS8427 (U5) to generate the necessary clocks.

In Slave Mode, for ADC operation, the ADCLRC_IN clock is derived from the DACLRC_OUT signal by connecting SMB connectors J9 and J22 together. The DACLRC_OUT signal is generated by the CS8427 (U5) when a digital signal as previously described is applied to J15 or U1.

A direct digital input is also available via one side of a 2x8 pin header (H1); data must be input in one of the WM8734 supported formats - see datasheet.

BOARD OUTPUT

The output interface from the board is via an optical (U6) or coaxial (J26) digital (AES/EBU, UEC958, S/PDIF, EIAJ CP340/1201) signal output. A direct signal output is available via one side of a 2x6 pin header (H2). Data is output in one of the WM8734 supported formats - see datasheet.

There are two analogue signal output phono connectors J25 (LOUT) and J21 (ROUT). These signals are AC coupled (optional, may be bypassed via links J20 and J24) before being output from the board. There is also an SMB connector J22 (DACLRC_OUT). This may be used to connect to some external circuit. DACLRC is only an output when the WM8734 is in Master Mode.

Warning: If AC coupling capacitors are bypassed, the outputs will be on a DC level (AVDD/2). This can damage Hi-Fi equipment if directly connected.

WM8734-EV2M

INTERFACES

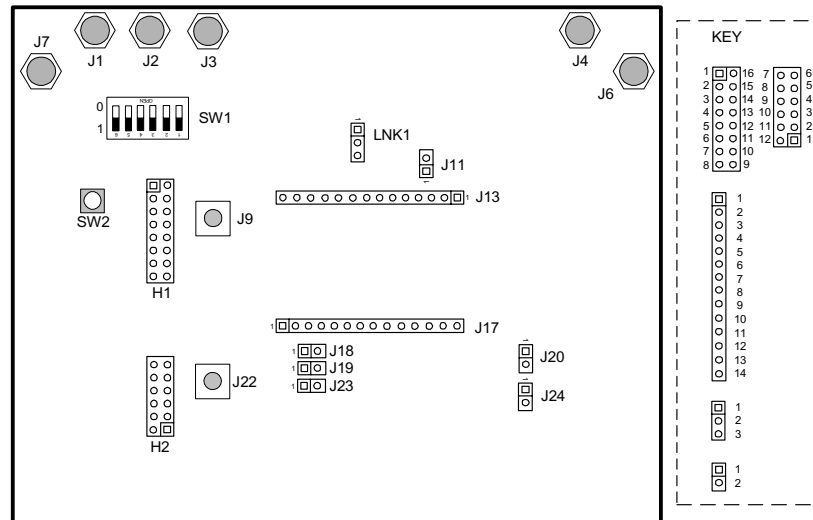


Figure 1 Interfaces

HEADERS

H1	SIGNAL
1/16	MCLK
2/15	GND
3/14	DACDAT
4/13	GND
5/12	BCLK
6/11	GND
7/10	DACLR
8/9	GND

H2	SIGNAL
7/6	GND
8/5	ADCDAT
9/4	GND
10/3	BCLK_OUT
11/2	GND
12/1	ADC_LRC_OUT

J17	WM8734	SIGNAL
1	1	MCLK
2	2	NC
3	3	DCVDD
4	4	DGND
5	5	DBVDD
6	6	NC
7	7	BCLK
8	8	DACDAT
9	9	DACLR
10	10	ADCDAT
11	11	ADCLR
12	12	NC
13	13	NC
14	14	NC

J13	WM8734	SIGNAL
1	15	NC
2	16	LOUT
3	17	ROUT
4	18	AVDD
5	19	AGND
6	20	VMID
7	21	NC
8	22	NC
9	23	RLINEIN
10	24	LLINEIN
11	25	MODE
12	26	CSB
13	27	SDIN
14	28	SCLK

Table 2 Headers

LINK AND JUMPERS

LINKS & JUMPERS	LINK STATUS	DESCRIPTION
LNK1	Pins 1 & 2 SHORT Pins 2 & 3 SHORT	External source select (i.e. SPDIF input) No effect
J11	OPEN SHORT	SPI software interface control 2-wire software interface control
J20	OPEN SHORT	ROUT signal is AC coupled ROUT signal with no AC coupling ¹
J24	OPEN SHORT	LOUT signal is AC coupled LOUT signal with no AC coupling ¹
J18 (BCLK)	OPEN SHORT	Master mode Slave mode
J19 (DACLRC)	OPEN SHORT	Master mode Slave mode
J23 (ADCLRC)	OPEN SHORT	Master mode Slave mode
J9	Short to J22 in ADC Slave mode	ADCLRC input for slave mode ²
J22	Short to J9 in ADC Slave mode	DACLRC output used for external sync for ADC in Slave Mode ²

Table 3 Links

Note:

1. Caution: Output signals in this configuration will be DC biased to AVDD/2.
2. When running the ADC in slave mode ADCLRC and MCLK can be generated from a correctly formatted digital input on J15 or U1. LNK1 must be in position 1-2, and J9 and J22 linked together for this to be achieved.

SWITCHES

SWITCH	1	2	3	4	5	6	DATA FORMAT
SW1 (Data Format)	1	0	0	1	0	0	I2S Compatible
	1	0	0	0	0	1	24-bit Right Justified
	1	0	0	0	0	0	Left Justified
SW2 (Reset)	After an input data format change has been made using SW1, the CS8427 will only latch the new settings after SW2 has been pressed and released.						

Table 4 Switches

WM8734 OPERATION

SOFTWARE CONTROL

There are two possible serial control modes that may be selected to operate the WM8734. The standard SPI user interface is a 3-wire solution with the second option being a 2-wire solution.

3-WIRE MODE

To operate the WM8734 in SPI (3-wire) mode, the jumper on link J11 must be removed leaving pins 1 and 2 OPEN. The 3-wire serial interface then becomes active on pins 28(SCLK), 27(SDIN) and 26(CSB). The serial interface on the board can be connected to a PC via the printer port or any other standard parallel port. The port used can be selected through the software provided. The software supplied with this kit gives the user access to all the possible features provided by the WM8734. The 3-wire latch, data and clock lines may also be connected to the board via the test points TP3 (CSB), TP2 (SDIN) and TP1 (SCLK).

Please refer to the WM8734 datasheet for full details of the serial interface timing and all register features.

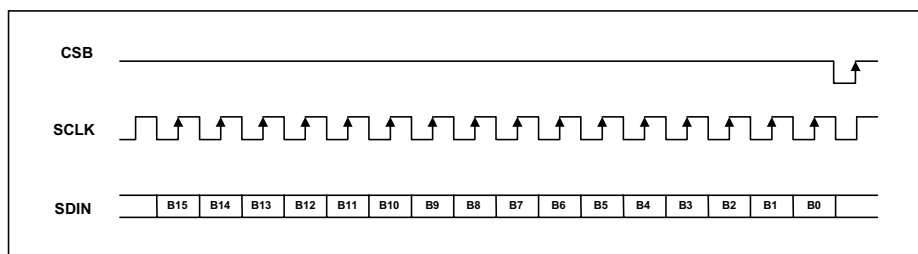


Figure 2 3-Wire Serial Interface

2-WIRE MODE

To operate the WM8734 in 2-wire mode, the jumper on link J11 must SHORT pins 1 and 2. The 2-wire serial interface becomes active on pins 28(SCLK) and 27(SDIN). The serial interface on the board can be connected to a PC via the printer port or any other standard parallel port. **Note: a bi-directional parallel port is required for 2-wire operation¹.** The 2-wire data and clock lines may also be connected to the board via the test points TP2 (SDIN) and TP1 (SCLK).

When used in 2-wire mode, the WM8734 has two possible addresses (0011010 [0x34h] or 0011011 [0x36h]) that are selectable by pulling CSB low or high. If connecting a probe to the Test Points it must be noted that the CSB line is pulled high on the WM8734 evaluation board selecting address 0011011. CSB must be pulled low or driven low through the software writes if address 0011010 is used (as is done in the WM8734-EV2S software provided).

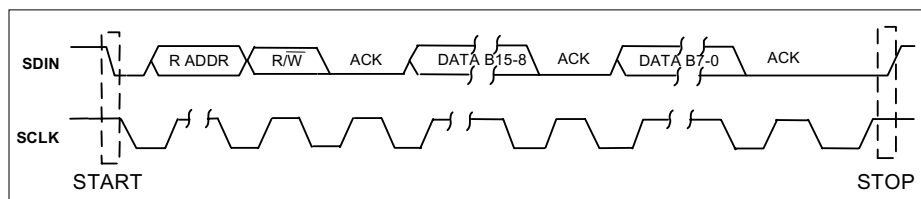


Figure 3 2-Wire Serial Interface

Note:

If the 2-wire mode is not reporting as expected then the most likely cause is that the parallel port being used is not bi-directional. In most PC's, the parallel port can be configured in the BIOS settings during initial power up.

Register	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R0 (00h)	0	0	0	0	0	0	0	LRIN BOTH	LIN MUTE	0	0	LINVOL				
R1 (02h)	0	0	0	0	0	0	1	RLIN BOTH	RIN MUTE	0	0	RINVOL				
R4 (08h)	0	0	0	0	1	0	0	0	0	0	0	DAC SEL	0	0	0	0
R5 (0Ah)	0	0	0	0	1	0	1	0	0	0	0	HPOR	DAC MU	DEEMPH		ADC HPD
R6 (0Ch)	0	0	0	0	1	1	0	0	PWR OFF	1	1	OUTPD	DACPD	ADCPD	1	LINEIN PD
R7 (0Eh)	0	0	0	0	1	1	1	0	BCLK INV	MS	LR SWAP	LRP	IWL		FORMAT	
R8 (10h)	0	0	0	1	0	0	0	0	0	CLKI DIV2	SR				BOSR	USB/ NORM
R9 (12h)	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	ACTIVE
R15(1Eh)	0	0	0	1	1	1	1	RESET								
	ADDRESS							DATA								

Table 5 Mapping of Program Registers

Please refer to the WM8734 datasheet for full details of the serial interface timing and all register features.

SERIAL INTERFACE SOFTWARE DESCRIPTION

SOFTWARE INSTALLATION

There are 2 floppy disks supplied with this evaluation kit. To install the software:

1. Insert disk 1
2. Select the 'Start' button on the Windows task bar and the 'Run...' option.
3. Type "A:\set-up" and then press OK.
4. Follow the on-screen instructions.

SOFTWARE OPERATION



Figure 4 WM8734 Default Screen Settings

The WM8734 default screen settings shown in Figure 4 resemble the default state of the device at initial power on. After a device Reset the 'WM8734' button can be pressed to set the software interface to match the WM8734 register values. Pressing the 'WM8734' button does not write to the WM8734, it only changes the software screen settings.

Important: It must be noted that the CS8427 SPDIF decoder IC will only work at a rate of 256fs. This will limit the sample rates that may be set using the WM8734 unless an external source is used supplying signals directly to the relevant pins of header H1 or taking the signals from the relevant pins of header H2.

DAC DEFAULT SET-UP

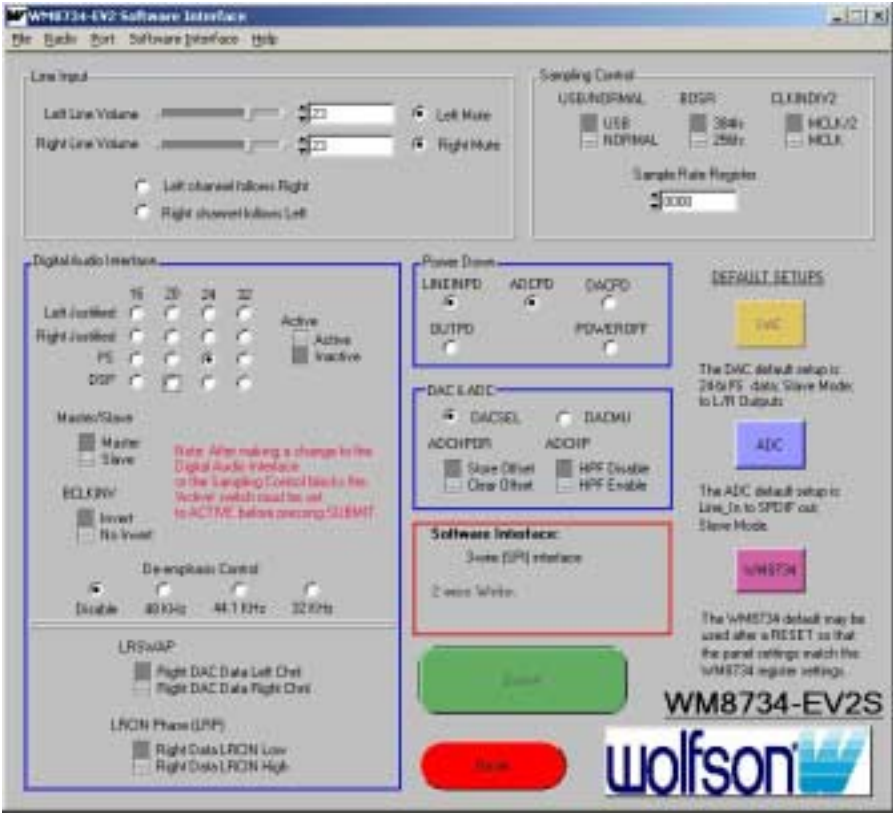


Figure 5 DAC Default Screen Settings

By pressing the DAC default button, the software writes to the device setting the SPDIF_In through DAC to Line_Out & HP_Out paths active in 24-bit, I²S input data format. This is to ease the initial use of the WM8734 until the user becomes familiar with both device and software operation.

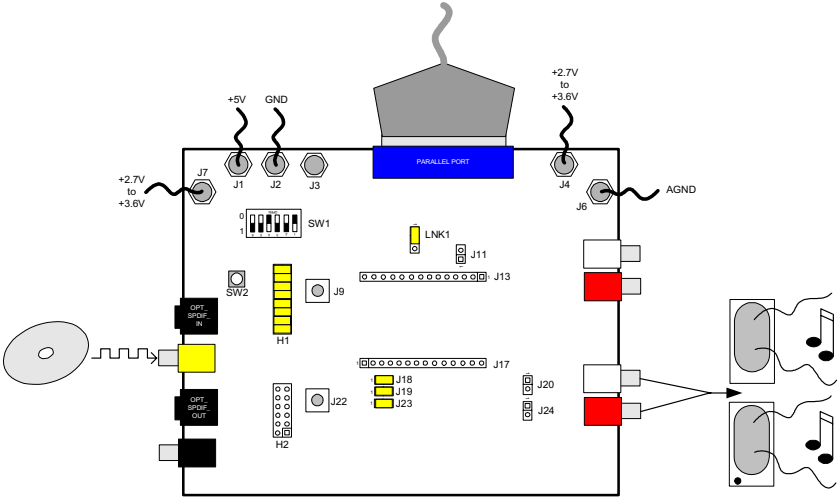


Figure 6 WM8734-EV2B Board Setup for DAC Operation

WM8734-EV2M

Note:

Setup for Slave Mode; SPI software control mode; I²S data format operation. The WM8734 registers must be set accordingly by pressing the DAC button as described above.

LINKS & JUMPERS	LINK STATUS	DESCRIPTION
LNK1	Pins 1 & 2 SHORT	External source select (i.e. SPDIF input)
J11	OPEN	SPI software interface control
J20	OPEN	ROUT signal is AC coupled
J24	OPEN	LOUT signal is AC coupled
J18 (BCLK)	SHORT	Slave mode
J19 (DACLR)	SHORT	Slave mode
J23 (ADCLRC)	SHORT	Slave mode
H1	All opposite pins SHORT	Digital audio interface input (DAC) signals
H2	All opposite pins OPEN	Digital audio interface output (ADC) signals

Table 6 DAC Test Jumper Setup (Slave Mode)

ADC DEFAULT SET-UP

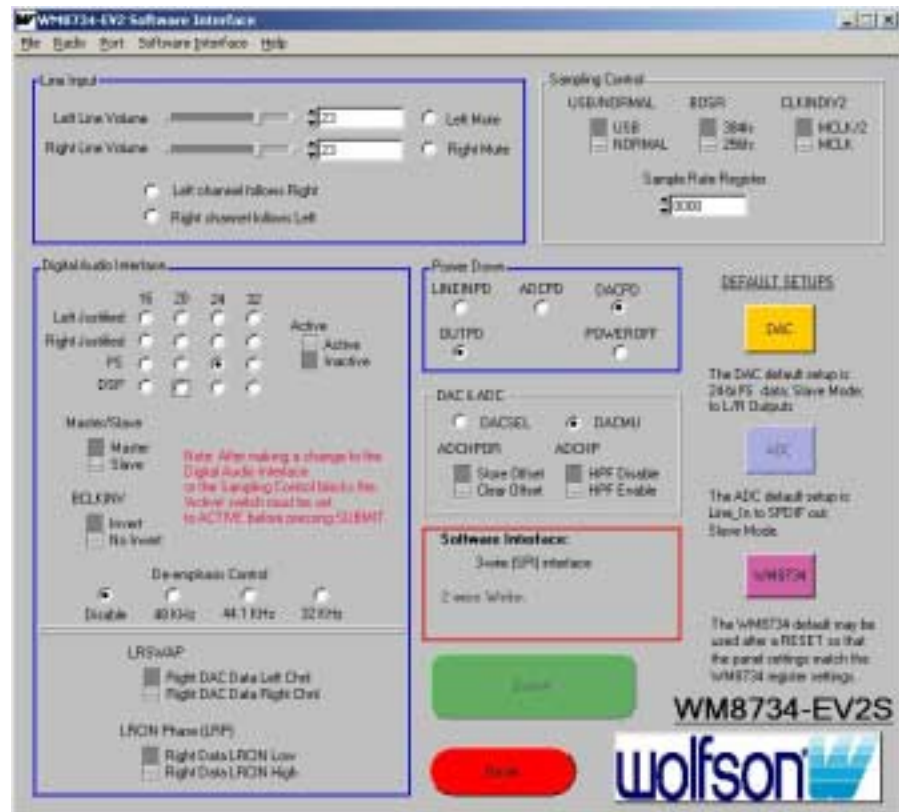


Figure 7 ADC Default Screen Settings

By pressing the ADC default button, the software writes to the device setting the Line_In through ADC to SPDIF_Out path active. This is to ease the initial use of the WM8734 until the user becomes familiar with both device and software operation.

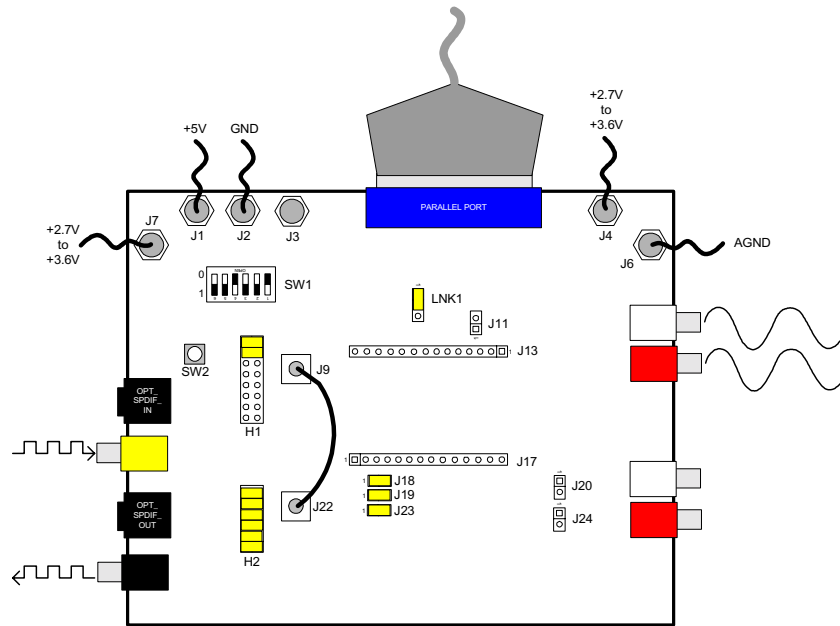


Figure 8 WM8734-EV2B Board Setup for ADC Operation

Note:

Setup for Slave Mode; SPI software control mode; I²S data format operation. The WM8734 registers must be set accordingly by pressing the ADC button as described above.

LINKS & JUMPERS	LINK STATUS	DESCRIPTION
LNK1	Pins 1 & 2 SHORT	External source select (i.e. SPDIF input)
J11	OPEN	SPI software interface control
J20	OPEN	ROUT signal is AC coupled
J24	OPEN	LOUT signal is AC coupled
J18 (BCLK)	SHORT	Slave mode
J19 (DACLRC)	SHORT	Slave mode
J23 (ADCLRC)	SHORT	Slave mode
H1	Pins 1&16; 2&15 are SHORT. All other pins are OPEN.	Digital audio interface input (DAC) signals
H2	All opposite pins SHORT	Digital audio interface output (ADC) signals
J9 & J22	SHORT	ADCLRC_IN to DAC_LRC_OUT for Slave Mode

Table 7 ADC Test Jumper Set-up (Slave Mode)

WM8734-EV2M

CHANGING THE DEFAULT SET-UP

If any further changes are made to the settings, after a default button is pressed, the Submit button must be pressed to write the new settings to the WM8734.



Figure 11 Changing Default Settings

Once any of the WM8734 default settings are changed on the control panel, the relevant section is highlighted (see Figure 11) to show the section where the setting has changed. For example, as shown in Figure 11, the Left and Right channel mutes have been unchecked. The highlight around the relevant section also has the purpose of letting the user know that they have not yet submitted the required changes to the WM8734. After a Submit, all the sections default back to their original 'panel grey' colour. The Submit button also becomes inactive until another change is made to the register settings.

All volume sliders are automatically submitted to the WM8734, and updated in "real-time".

If the WM8734 has been set active and a change is made to the Digital Audio Interface or the Sampling Control, the Active switch automatically goes to Inactive (as suggested in the WM8734 datasheet). This is to ensure that there are no digital interface issues caused by changes being made to these sections while the Active switch is in the 'Active' position.

MASTER MODE OPERATION

As well as being used in Slave mode as described in the default settings already mentioned, the WM8734 may be used in Master mode. When using any of the default setups, the WM8734 can be easily changed from a Slave to a Master device by writing to the WM8734 registers using the supplied software.

ADC NORMAL SETUP

To set the WM8734-EV2B into ADC Master mode, press the 'ADC' default button, change the 'Master/Slave' switch to Master and ensure that the 'Active' switch is set to the Active position. Then press the 'Submit' button. The board should be set up as shown in Figure 12 and Table 9.

Note:

The only digital signal that is supplied to the WM8734 audio interface is MCLK. All other signals are output from the WM8734 in Master Mode.

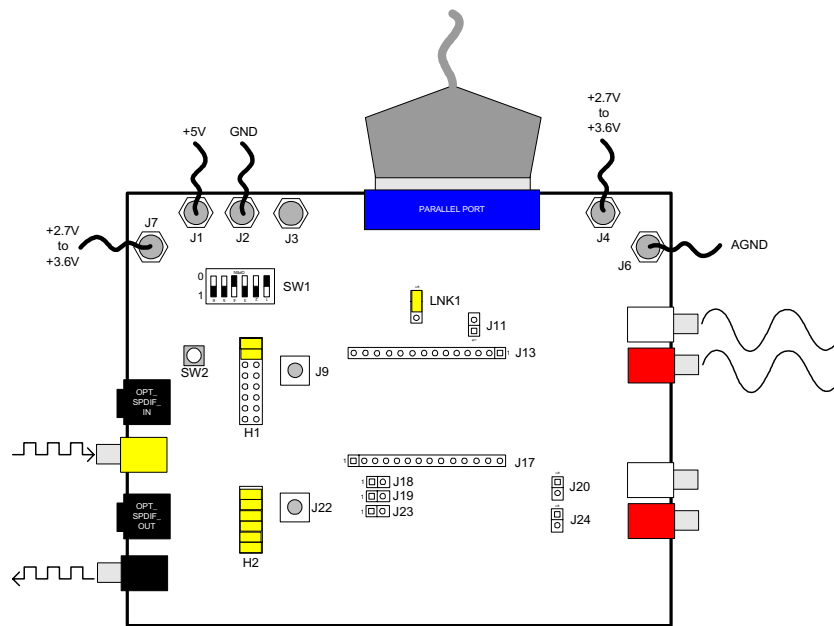


Figure 12 WM8734-EV2B Board Setup for ADC Operation in Master Mode

Note:

Setup for Master Mode; SPI software control mode. The relevant WM8734 registers must be set using the software.

WM8734-EV2M

LINKS & JUMPERS	LINK STATUS	DESCRIPTION
LNK1	Pins 1 & 2 SHORT	External source select (i.e. SPDIF input)
J11	OPEN	SPI software interface control
J20	OPEN	ROUT signal is AC coupled
J24	OPEN	LOUT signal is AC coupled
J18 (BCLK)	OPEN	Master mode
J19 (DACLRC)	OPEN	Master mode
J23 (ADCLRC)	OPEN	Master mode
H1	Pins 1&16; 2&15 are SHORT. All other pins are OPEN.	Digital audio interface input (DAC) signals
H2	All opposite pins SHORT	Digital audio interface output (ADC) signals

Table 9 ADC Normal Master Mode Set-up

SOFTWARE MENU FEATURES

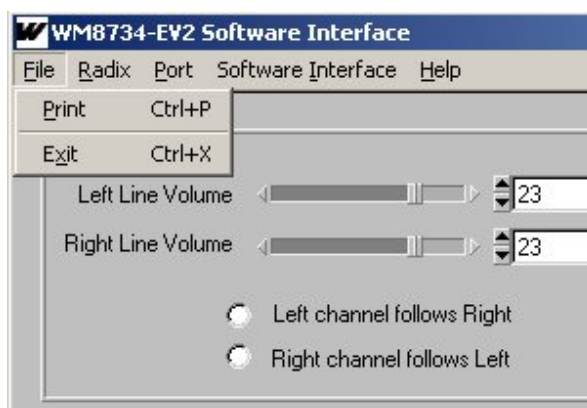


Figure 15 Options Available from the File Menu

Figure 15 shows the 'File' menu. This menu is used for printing the screen to the PC's default printer and to exit the WM8734 software.

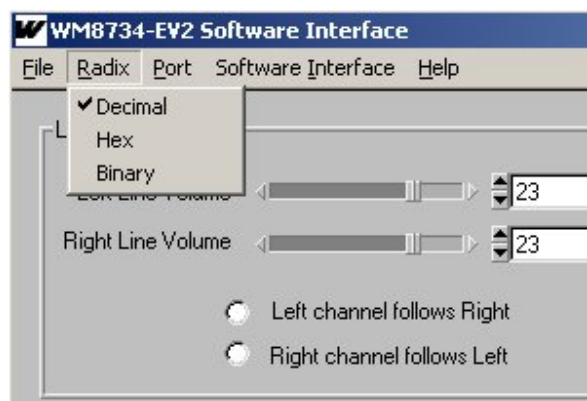


Figure 16 Options Available from the Radix Menu

The 'Radix' menu shown in Figure 16 allows the user to choose which numeric format to view the Line Input and Headphone Output volume control settings in.

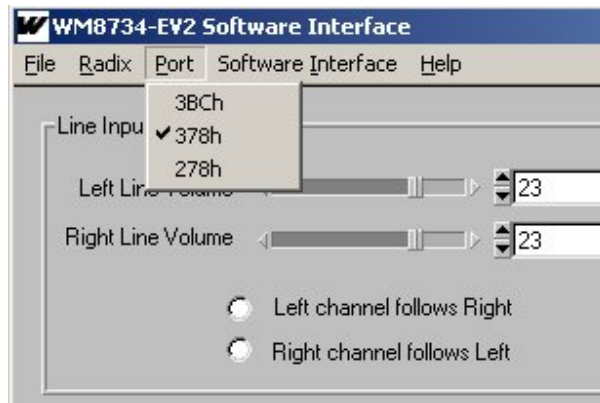


Figure 17 Options Available from the Port Menu

The 'Port' menu shown in Figure 17 allows the user to specify a parallel port address on the PC.

The 'Help' menu (not shown) gives the software version number and contact details if further assistance is required.



Figure 18 Options Available from the Software Interface Menu

The 'Software Interface' menu shown in Figure 18 allows the user to select which method of control is to be used. 3-wire (SPI) or 2-wire with a choice of two available addresses offered by the WM8734.

The current software control method is displayed in the box highlighted in red at the bottom of the software control window. In 2-wire mode, the result of the write is also displayed. As shown in Figure 19, an 'Error in Address' has been reported - Please refer to the WM8734 datasheet for a full explanation of 2-wire mode operation.

WM8734-EV2M

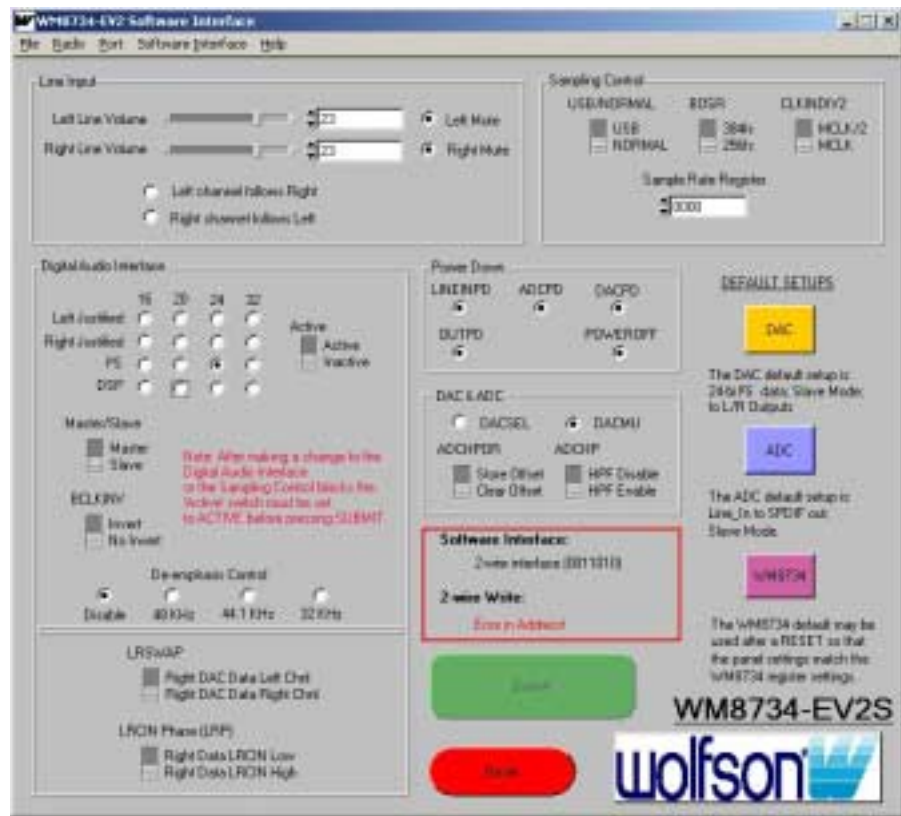


Figure 19 2-wire Interface Write Result

If clicked on, the Wolfson logo in the bottom left of the control panel window will open the Wolfson website (www.wolfsonmicro.com) in the PC's default browser.

WM8734-EV2B SCHEMATIC

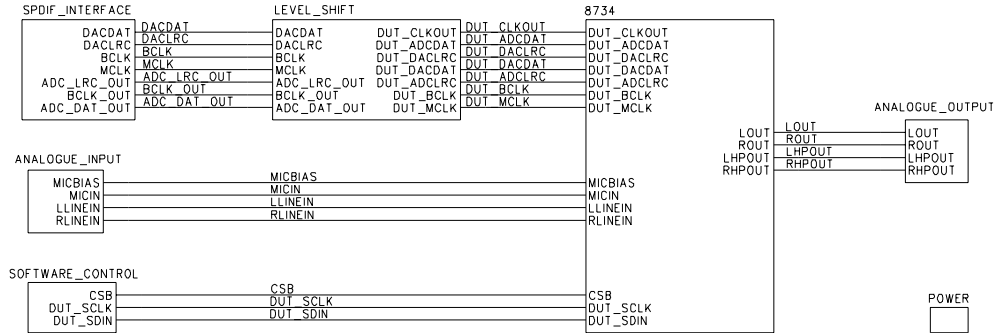


Figure 20 Functional Diagram

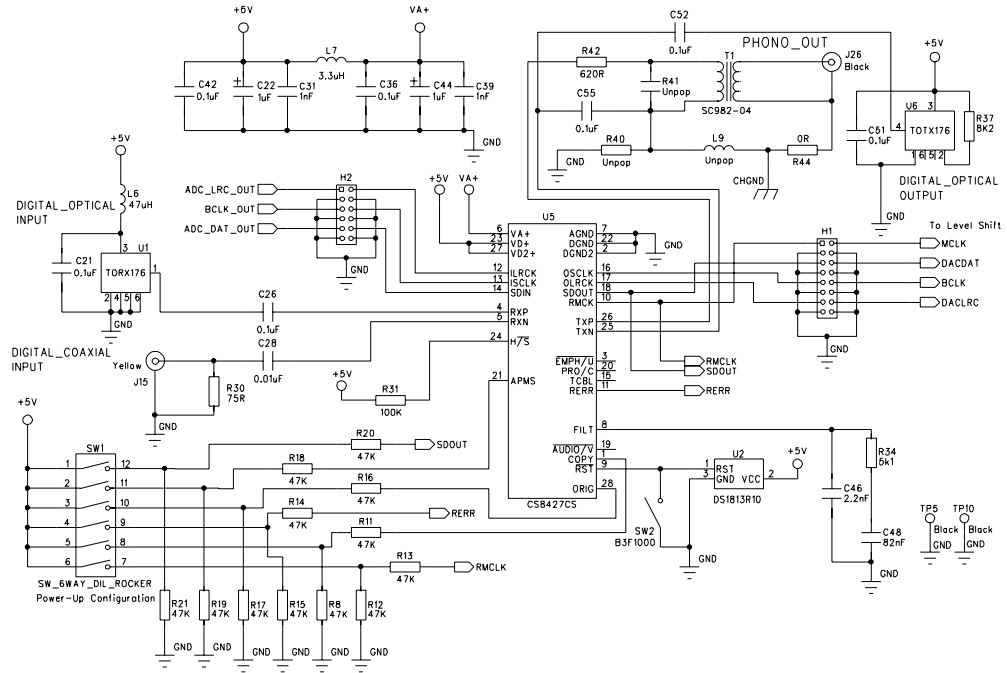


Figure 21 SPDIF Interface

WM8734-EV2M

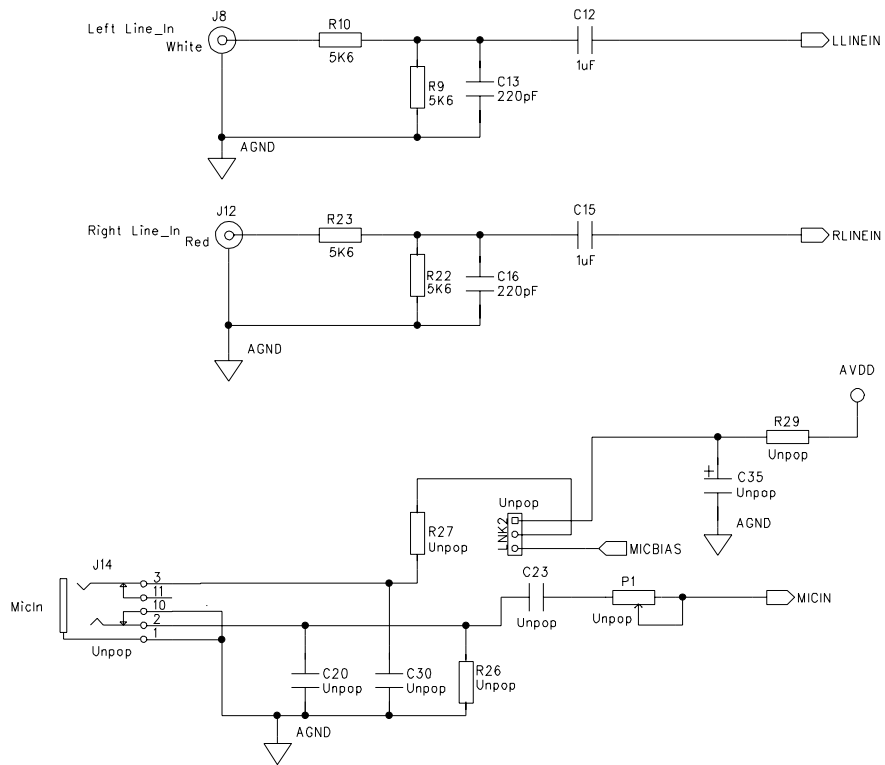


Figure 22 Analogue Input

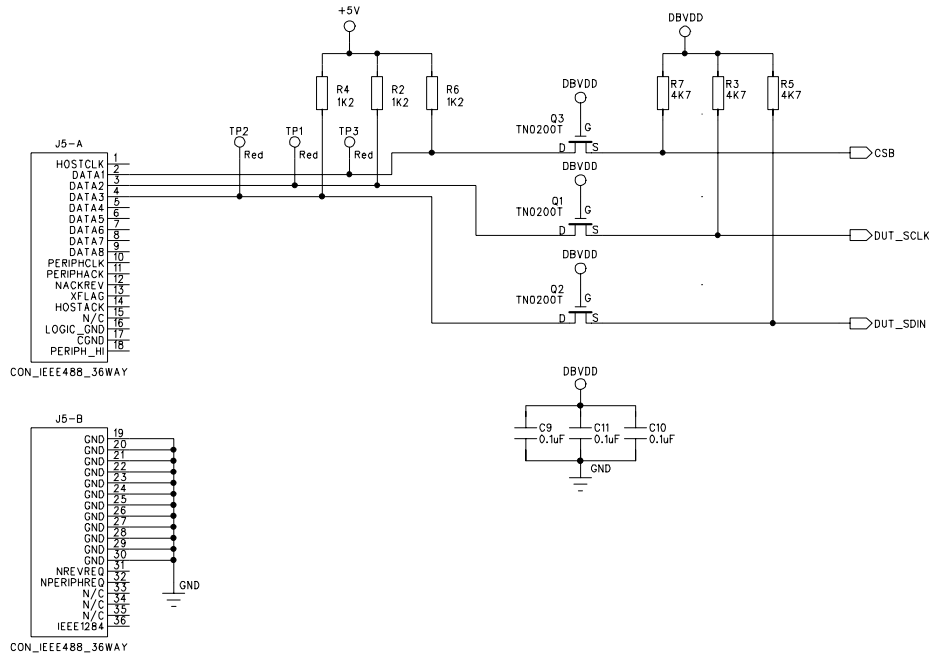


Figure 23 Software Control

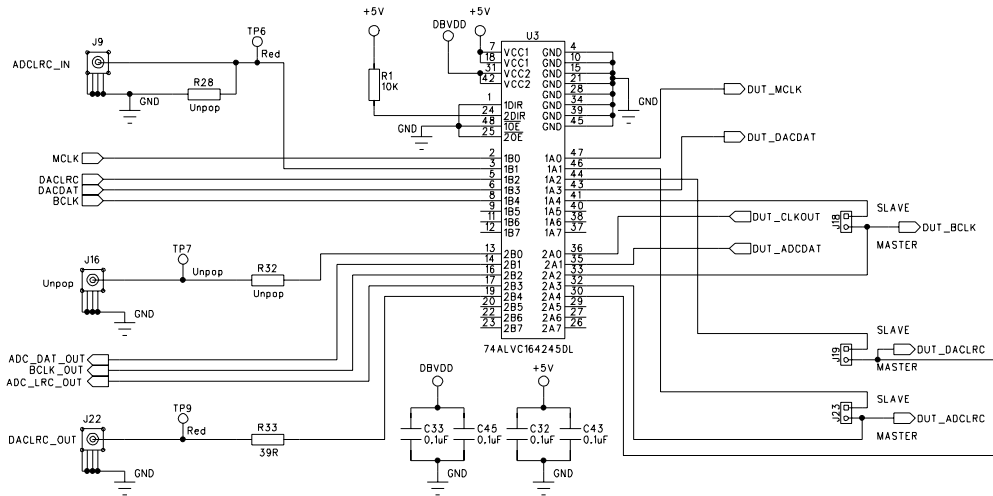


Figure 24 Level Shift

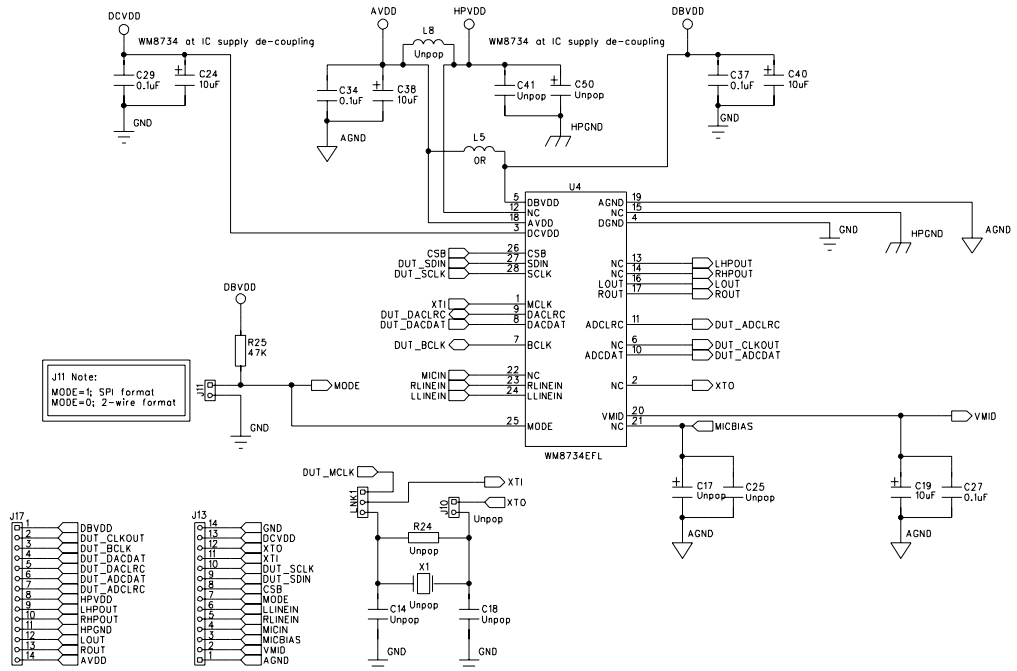


Figure 25 WM8734

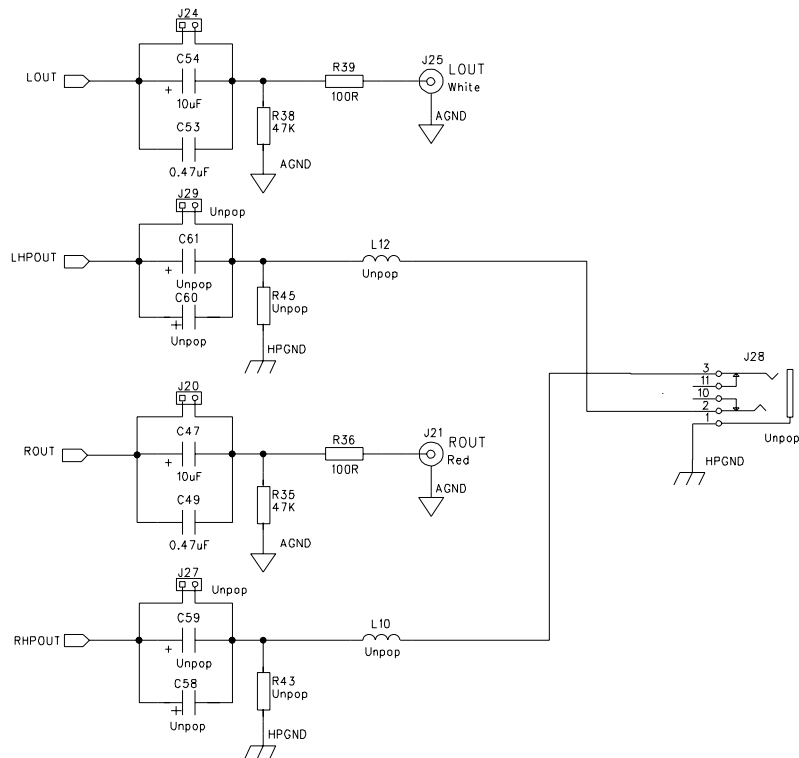


Figure 26 Analogue Output

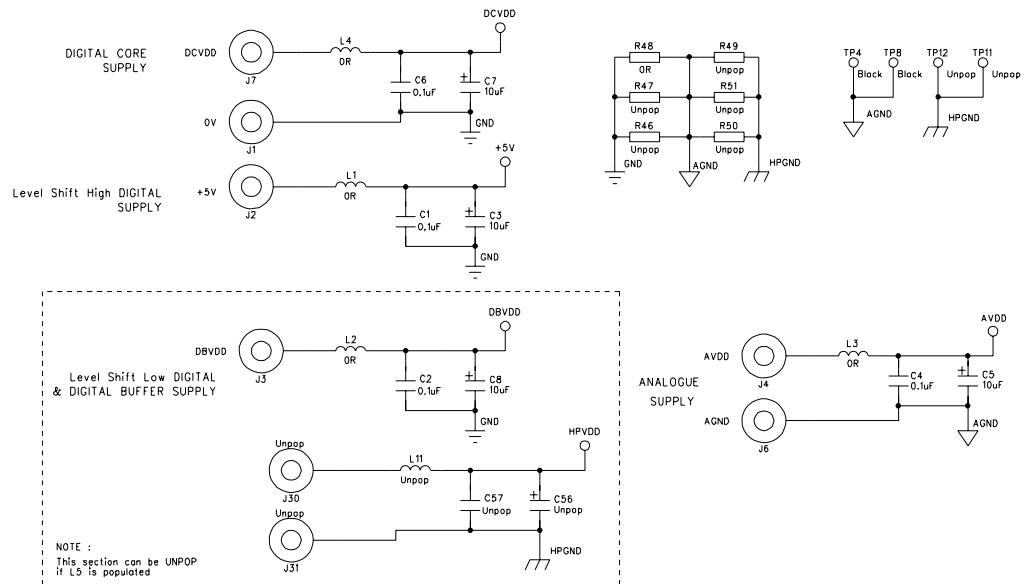


Figure 27 Power

WM8734-EV2B PCB LAYOUT

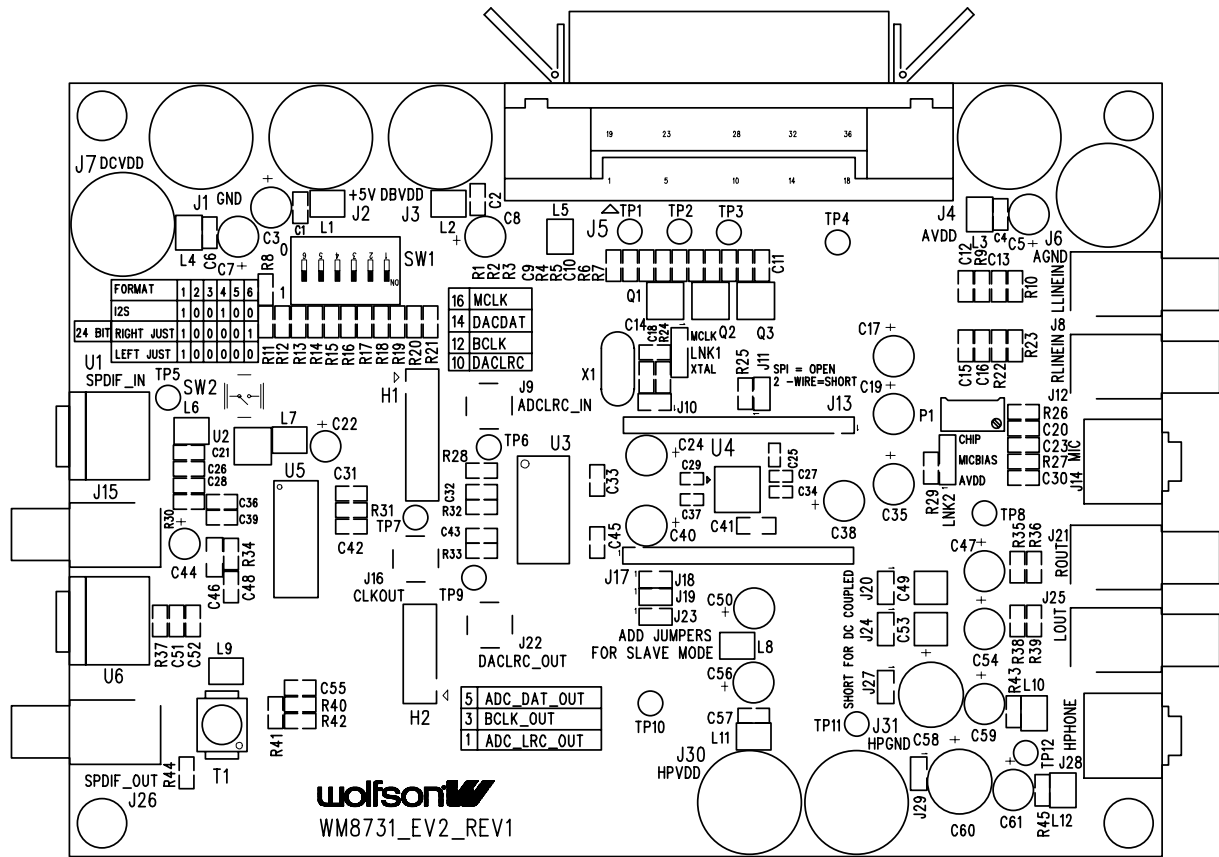


Figure 28 Top Layer Silkscreen

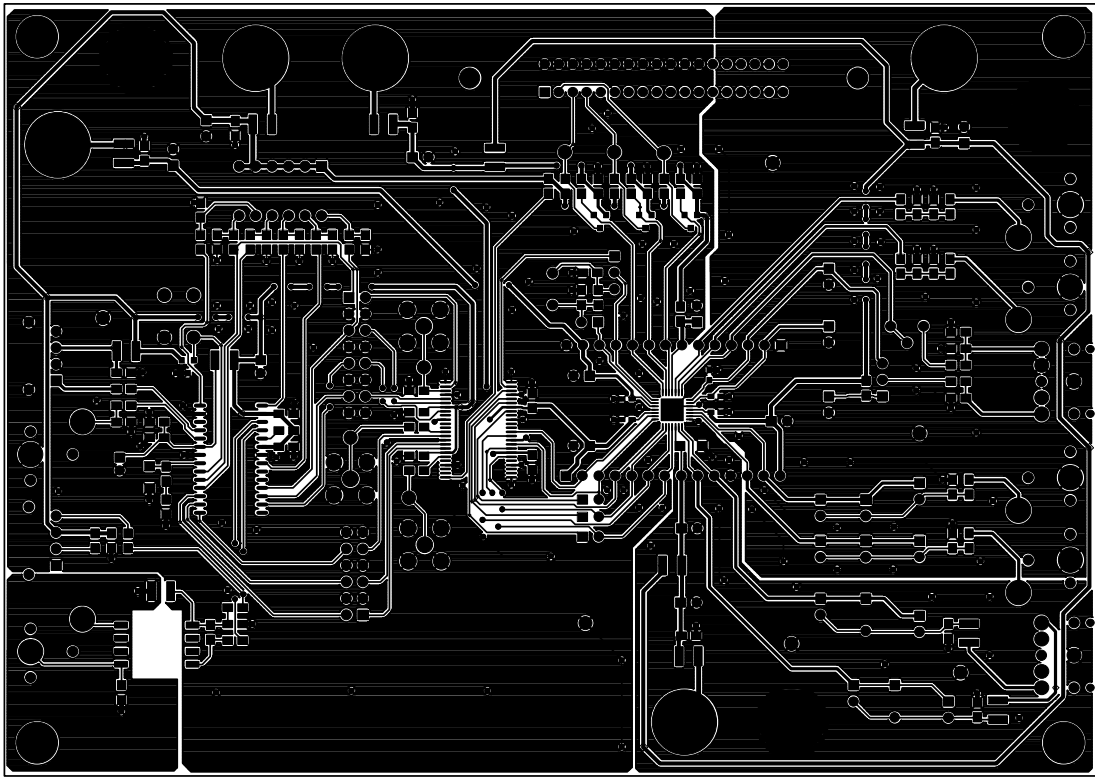


Figure 29 Top Layer

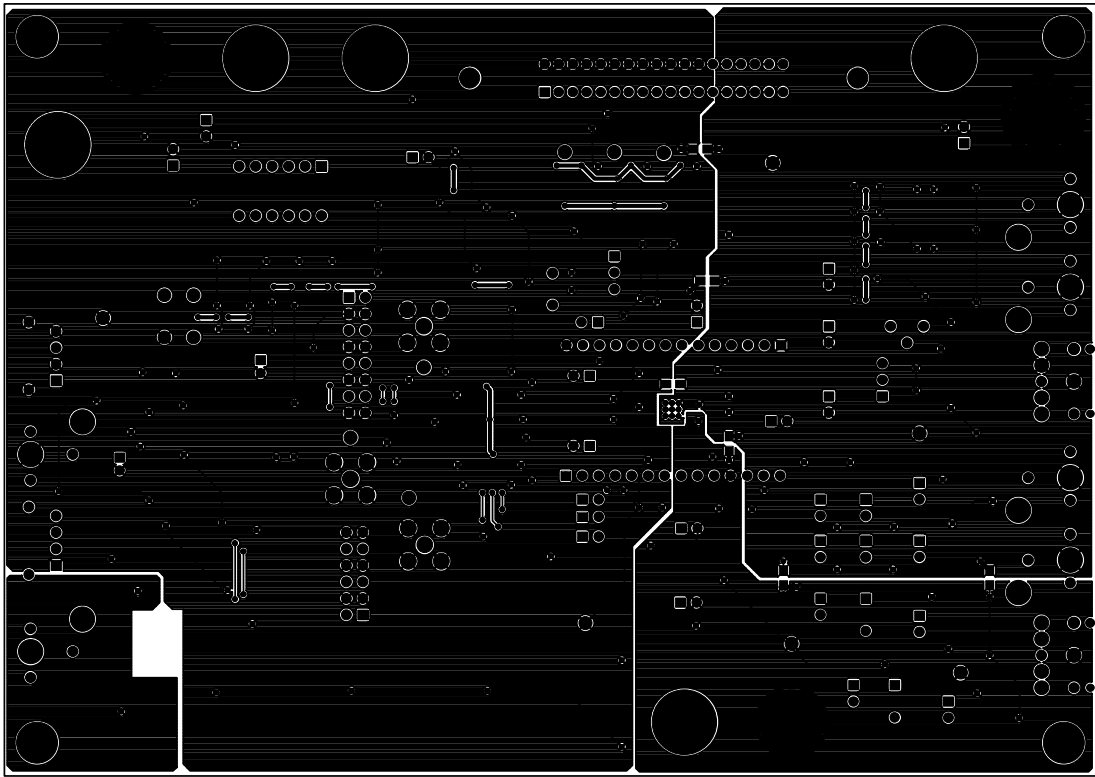


Figure 30 Bottom Layer

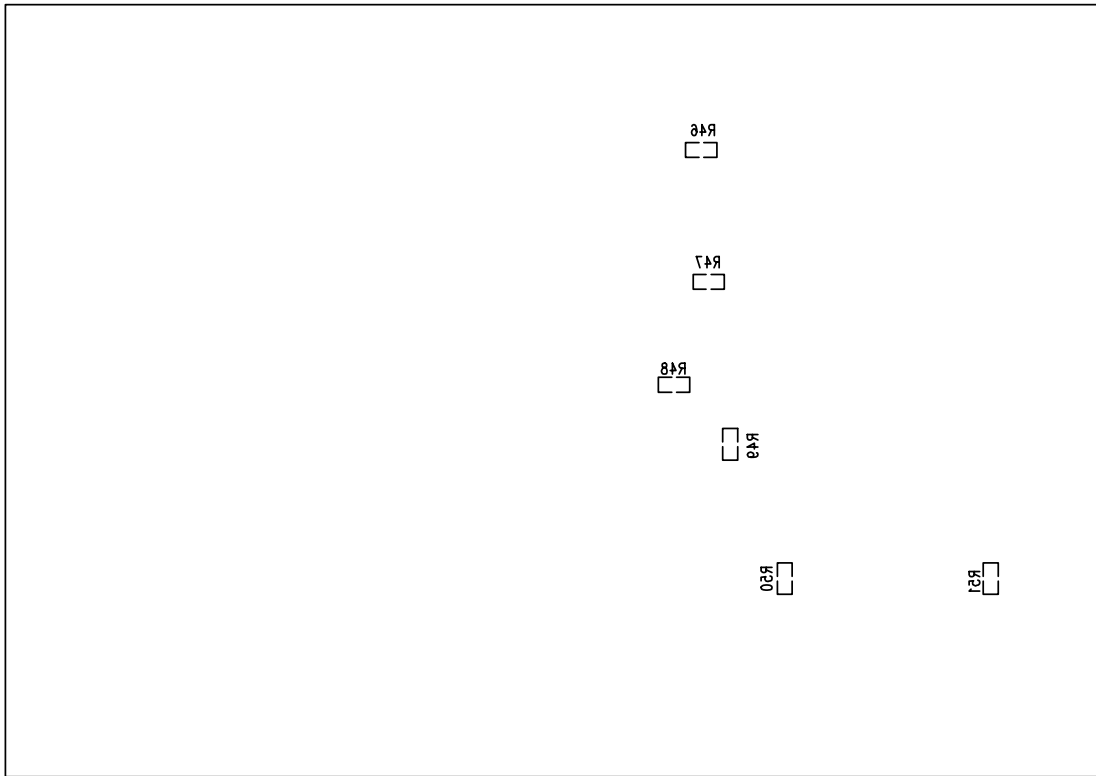


Figure 31 Bottom Layer Silkscreen

WM8734-EV2B BILL OF MATERIAL

Description	REF-DES	QTY
0.01uF 0805 SMD Ceramic Capacitor 50V X7R	C28	1
0.1uF 0603 SMD Ceramic Capacitor 16V X7R	C27 C29 C34 C37	4
0.1uF 0805 SMD Ceramic Capacitor 50V X7R	C1-2 C4 C6 C9-11 C21 C26 C32-33 C36 C42-43 C45 C4	18
0.47uF MKS02 leaded Polyester Capacitor 50V 20%	C49 C53	2
0R 0805 SMD chip resistor 1% 0.1W	R44 R48	2
0R 1206 Resistor on 1210 Inductor site	L1-5	5
1.32mm PCB Test Terminal BLACK	TP4-5 TP8 TP10	4
1.32mm PCB Test Terminal RED	TP1-3 TP6 TP9	5
1.32mm PCB Test Terminal UNPOP	TP7 TP11-12	3
100K 0805 SMD chip resistor 1% 0.1W	R31	1
100R 0805 SMD chip resistor 1% 0.1W	R36 R39	2
10K 0805 SMD chip resistor 1% 0.1W	R1	1
10uF 6.3 Dia 2.5 pitch Oscon Through Hole Cap. 16V 20%	C3 C5 C7-8 C19 C24 C38 C40 C47 C54	10
12 MHz HC49-4H 3.5mm 30pF Crystal	X1	1
1K2 0805 SMD chip resistor 1% 0.1W	R2 R4 R6	3
1nF 0805 SMD Ceramic Capacitor 50V NPO	C31 C39	2
1uF 0805 SMD Ceramic Capacitor 10V X7R	C12 C15	2
1uF 4 Dia 2 pitch Oscon Through Hole Cap. 25V 20%	C22 C44	2
1x14 2.54mm pitch PCB Pin Header VERTICAL	J13 J17	2
1x2 PCB Pin Header 0.1" VERTICAL	J11 J18-20 J23-24	6
1x2 PCB Pin Header 0.1" VERTICAL UNPOP	J10 J27 J29	3
1x3 PCB Pin Header 0.1" VERTICAL	LNK1	1
1x3 PCB Pin Header 0.1" VERTICAL UNPOP	LNK2	1
2.2nF 1206 SMD Ceramic Capacitor 50V NPO	C46	1
2:1 Ratio 96KHz SPDIF Digital Audio transformer SOIC	T1	1
220pF 0805 SMD Ceramic Capacitor 50V X7R	C13 C16	2
2x6 2.54mm pitch PCB Pin Header VERTICAL	H2	1
2x8 2.54mm pitch PCB Pin Header VERTICAL	H1	1
3.3uH 1210 Surface Mount Inductor '1210A series'	L7	1
3.5mm Jack Socket UNPOP	J14 J28	2
36-way Centronics/IEE488 PCB mountable Connector	J5	1
39R 0805 SMD chip resistor 1% 0.1W	R33	1
47K 0805 SMD chip resistor 1% 0.1W	R8 R11-21 R25 R35 R38	15
47uH 1210 Surface Mount Inductor 'PA series'	L6	1
4K7 0805 SMD chip resistor 1% 0.1W	R3 R5 R7	3
4mm Non-Insulated Panel Socket 16A	J1-4 J6-7	6
4mm Non-Insulated Panel Socket Unpop	J30-31	2
5k1 0805 SMD chip resistor 1% 0.125W	R34	1
5K6 0805 SMD chip resistor 1% 0.1W	R9-10 R22-23	4
620R 0805 SMD chip resistor 1% 0.1W	R42	1
74ALVC164245 16 Bit Dual Supply Bus Transceiver SO	U3	1
75R 0805 SMD chip resistor 1% 0.125W	R30	1
82nF 0805 SMD Ceramic Capacitor 25V X7R	C48	1
8K2 0805 SMD chip resistor 1% 0.1W	R37	1
B3F1000 SPNO PCB mount switch	SW2	1
CS8427 96KHz Audio Transceiver	U5	1
DIL Switch 6-Way Rocker	SW1	1
DS1813 5V active Low Power-On-Reset chip SOT	U2	1

WM8734-EV2M

Phono Socket PCB mount RED	J12 J21	2
Phono Socket PCB mount WHITE	J8 J25	2
Phono Socket PCB mount YELLOW	J15	1
Phono Socket PCB mount BLACK	J26	1
SMB Connector PCB Mount 50 Ohm VERTICAL	J9 J22	2
TN0200T N- Channel MOSFET SOT23	Q1-3	3
TORX176 Digital Audio Optical Receiver	U1	1
TOTX176 Digital Audio Optical Transmitter	U6	1
Unpop 0603 SMD Capacitor site	C25	1
Unpop 0805 SMD Ceramic Capacitor site	C14 C18 C20 C23 C30 C57 R41	7
Unpop 1206 SMD Ceramic Capacitor site	C41	1
Unpop 1210 Surface Mount Inductor site	L8-12	5
UNPOP 3296Y Potentiometer	P1	1
Unpop SMB Connector PCB Mount	J16	1
Unpopulated 0805 resistor site	R24 R26-29 R32 R40 R43 R45-47 R49-51	14
Unpopulated 10 Dia 5 pitch Through Hole Cap. site	C58 C60	2
Unpopulated 6.3 Dia 2.5 pitch Through Hole Cap. site	C17 C35 C50 C56 C59 C61	6
WM8734 Audio codec QFN	U4	1

Table 11 Board Bill Of Materials

Note:

1. The audio transformer used on this board is manufactured by Scientific Conversion Inc. (www.scientificconversion.com).

APPENDIX A

EXTERNAL DSP CONNECTION TO THE WM8734-EV2B

The WM8734-EV2B evaluation board has been designed to allow it to be easily connected to an external DSP platform with error free operation.

The following information is provided to ease the connection process and ensure that all signals sent and received by the WM8734-EV2B are reliable and at the correct voltage levels.

AUDIO INTERFACE CONNECTIONS

It is recommended that twisted pair (signal twisted with GND) or shielded wires are used to make the audio interface connections between the DSP and WM8734-EV2B platforms. This is to ensure that no interference or noise is picked up by the clocks or data lines, thus reducing performance and reliability.

When the WM8734 is set in **Slave Mode**, the jumpers on header H1 should be removed, disconnecting the digital input section of the evaluation board. The audio interface timing and data signals from the DSP platform should then be connected as shown in Figure 32. The signals should be connected to H1 and not on the header strips J13 and J17 running up each side of the device. Connecting the signals on the output side of the level-shift IC (U3) will cause drive contention between U3 and the DSP and could result in damage to either or both devices. In most cases, the DSP supplies will be set around 3V for low power portable applications. The inputs to the level-shift IC (74ALVC164245) have a TTL threshold (i.e. Logic High = +2V(min); Logic Low = +0.8V(max)) and low input current requirements (i.e. 15uA max) allowing most DSP's to connect directly.

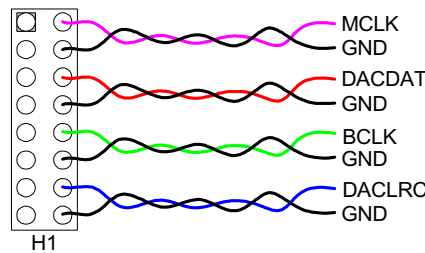


Figure 32 Connections from DSP Platform

The digital inputs to the WM8734 have a CMOS threshold (i.e. Logic High (min) = DBVDDx0.7; Logic Low (max) = DBVDDx0.3). These are met directly by the level shift IC outputs.

The jumpers on H2 should also be removed, disconnecting the digital output section of the WM8734 evaluation board. The ADCDAT data from the WM8734 should then be connected to the DSP via pin 6 of header strip J17 and the GND connection should be taken from pin 14 of header strip J13.

The ADCDAT signal should be taken direct from the WM8734 digital output as the output side of the level-shift IC (U3) from the WM8734 is pulled up to +5V which may overdrive and cause damage to the DSP inputs. The digital output levels of the WM8734 are Logic High (min) = DBVDDx0.9; Logic Low (max) = DBVDDx0.1 which should meet the input level requirements of most DSPs running at +3V supplies. If the DSP is running with +5V supplies then the connections to it should be made from the output side of the level-shift IC (U3), connecting the signals as shown in Figure 33.

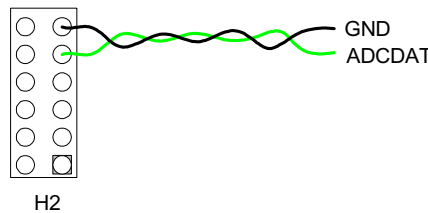


Figure 33 Data Connection to the DSP Platform (+5V tolerant input levels)

WM8734-EV2M

When the WM8734 is set to **Master mode**, the jumpers on header H1 should be removed, disconnecting the digital input section of the evaluation board. If an external MCLK signal is being used (i.e. supplied by the DSP) then the DSP platform should be connected as shown in Figure 34. The signal should be connected to H1 and not on the header strip J13 running up the side of the device. Connecting the signal on the output side of the level-shift IC (U3) will cause drive contention between U3 and the DSP and could result in damage to either or both devices. In most cases, the DSP supplies will be set around +3V for low power portable applications. The inputs to the level-shift IC (74ALVC164245) have a TTL threshold (i.e. Logic High = +2V(min); Logic Low = +0.8V(max)) and low input current requirements (i.e. 15uA max) allowing most DSPs to connect directly.

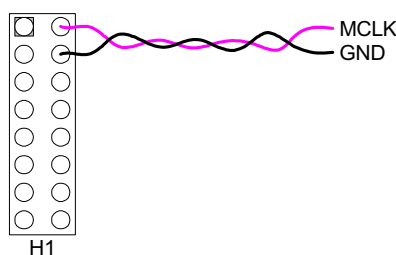


Figure 34 Timing Connections from DSP Platform

The digital inputs to the WM8734 have a CMOS threshold (i.e. Logic High (min) = $DBVDD \times 0.7$; Logic Low (max) = $DBVDD \times 0.3$). These are met directly by the level shift IC outputs.

The jumpers on H2 should also be removed, disconnecting the digital output section of the WM8734 evaluation board. The ADCDAT, BCLK and ADCLRC signals from the WM8734 should then be connected to the DSP from headers J13 and J17 running up each side of the WM8734.

The ADCDAT, BCLK and ADCLRC signals should be taken direct from the WM8734 digital output as the output side of the level-shift IC (U3) from the WM8734 is pulled up to +5V which may overdrive and cause damage to the DSP inputs. The digital output levels of the WM8734 are Logic High (min) = $DBVDD \times 0.9$; Logic Low (max) = $DBVDD \times 0.1$ which should meet the input level requirements of most DSPs running at +3V supplies. If the DSP is running with +5V supplies (and +5V tolerant inputs) then the connections from the WM8734 evaluation board to the DSP should be made from H2 on the output side of the level-shift IC from the WM8734 as shown in Figure 35.

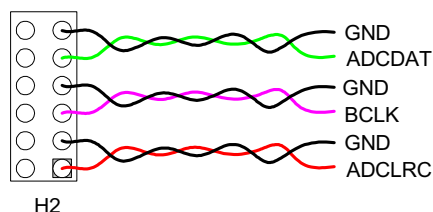


Figure 35 Connections to the DSP Platform (+5V tolerant input levels)

This will ensure that the DSP input level specifications are met.

SOFTWARE INTERFACE

When using the WM8734-EV2B evaluation board with a DSP platform, the registers may be set using the supplied software with a PC and parallel port cable as shown in Figure 36.

If the DSP is being used to write to the WM8734 registers as well as supplying/receiving the audio interface timing and data signals, then it is recommended that twisted pair or shielded wires are used to connect the DSP platform to the WM8734-EV2B. If the DSP supplies are set to the same voltage as the DBVDD supplies of the WM8734; a direct connection can be made to pin 8 (CSB), pin 9 (SDIN) and pin 10 (SCLK) of header strip J13 for 3-wire software mode as shown in Figure 37. If the DSP is running at a higher voltage (e.g. +5V) than the WM8734, then the signals from the DSP platform should be connected to test points TP3 (CSB), TP2 (SDIN) and TP1 (SCLK). Connecting the higher voltage signals from the DSP to the test points will level shift them through the transistors down to the same level as the DBVDD supply as shown in Figure 38. This will ensure that the WM8734 input CMOS thresholds (i.e. Logic High (min) = $DBVDD \times 0.7$; Logic Low (max) = $DBVDD \times 0.3$) are met and no damage is done to the device.

The same connections apply for controlling the WM8734 via 2-wire software mode (i.e. only pin 9 (SDIN) and pin 10 (SCLK) of header strip J13 are used). Pin8 (CSB) can be pulled low on the board if device address 0011010 [0x34h] is required or pulled high address 0011011 [0x36h] is required.

CONNECTION DIAGRAMS

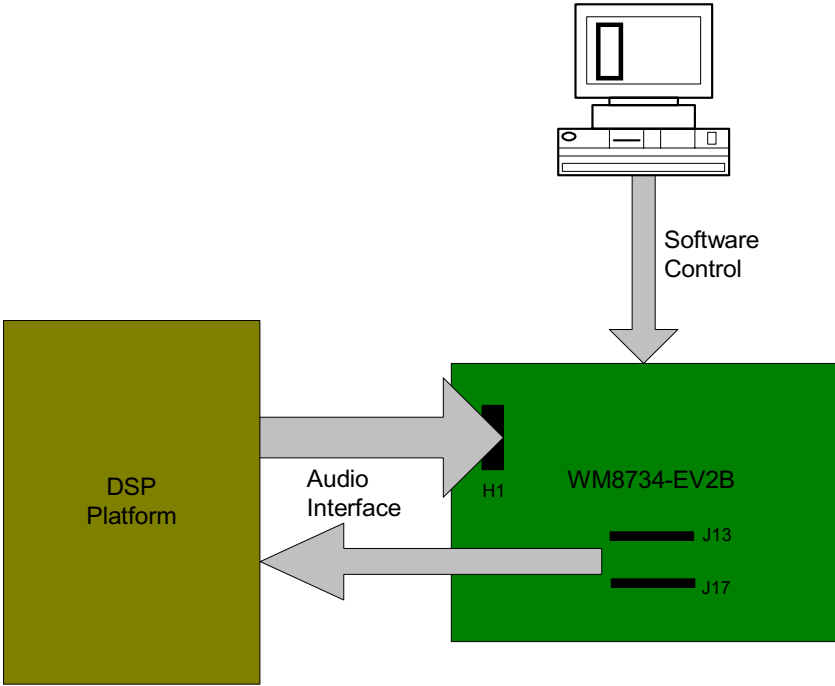


Figure 36 DSP Connection with PC Control using Wolfson Software

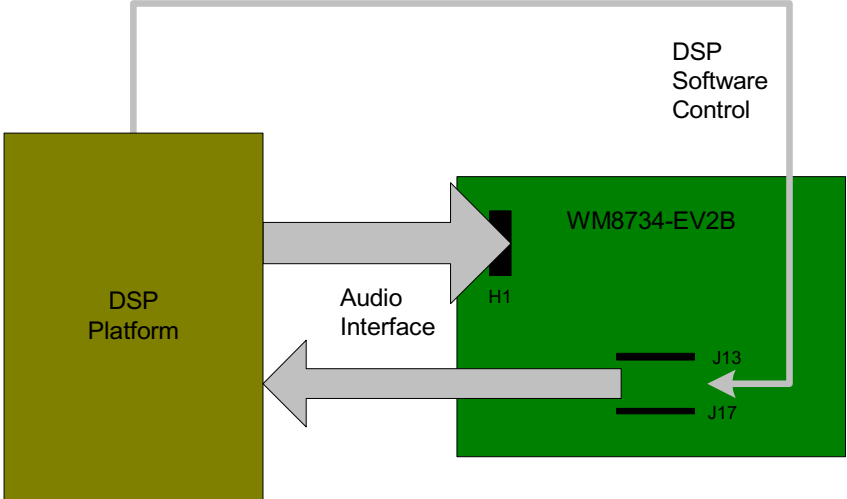


Figure 37 Full DSP Control with Equal Supplies for DSP and WM8734

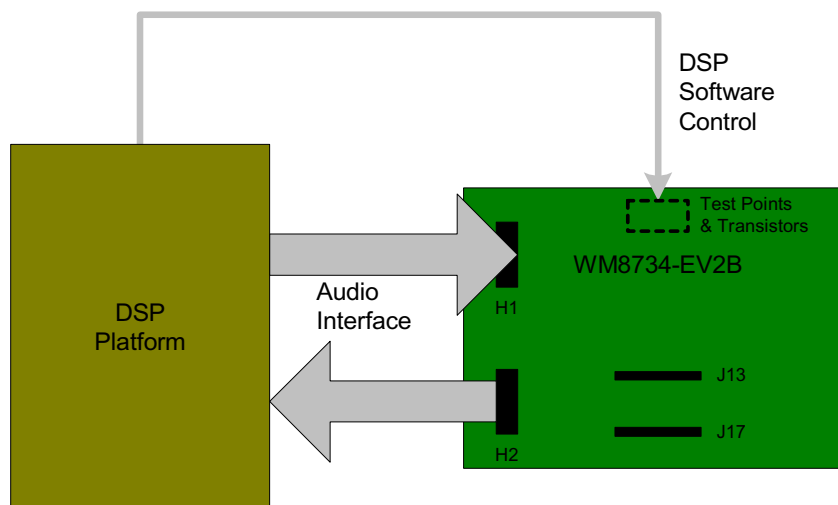


Figure 38 Full DSP Control with Higher DSP Supply than WM8734

EVALUATION SUPPORT

The aim of this evaluation kit is to help you to become familiar with the functionality and performance of the WM8734, stereo CODEC.

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

Email: apps@wolfsonmicro.com
Telephone Apps: (+44) 131 272 7070
Fax: (+44) 131 272 7001
Mail: Applications at the address on the last page.

or contact your local Wolfson representative.

Additional information may be made available from time to time on our web site at:
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