
Errata: CS4525 Rev. C1 Silicon

(Reference CS4525_DS726PP3 Data Sheet)

- ◆ In Software Mode, the total digital gain for each channel — including pre-scaler, tone control, parametric EQ, channel volume, and master volume — must not exceed +20 dB at any frequency.
- ◆ If the maximum voltage of VP can exceed 15.0 V, then the internal ramp feature must never be enabled and RmpSpd[1:0] must always be set to its default value of 11.
- ◆ The Thermal Foldback feature is disabled in Hardware Mode regardless of the state of the EN_TFB pin.
- ◆ If ADC input is selected, the Delay Port is enabled, and the Auxiliary Serial Output is configured for I2S format, then the Left and Right channels will be swapped on the AUX_SDOOUT output, the logic-level PWM_SIGx outputs, and the high-power OUTx outputs. To correct for this, it is recommended to set RChMix[1:0] to 11 and LChMix[1:0] to 11 to swap the signals.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to <http://www.cirrus.com>