WAN-0215

DRC Operation in Wolfson Audio CODECs

INTRODUCTION

This applications note has been created to explain the operation of the Dynamic Range Controller (DRC) used in the latest Wolfson audio CODECs. Not all devices will have all of the functions described in this application note. The devices using the DRC function are shown in Table 1.

WM8903	WM8904	WM8912	WM8944	WM8945	WM8946
WM8948	WM8993	WM8994			

Table 1 Devices that use the DRC Function

This list will change as newer devices are introduced using this same technology.

The DRC is a circuit that can be enabled in the playback or digital record path of the CODEC, depending upon the selected DSP mode, boost quiet signals and attenuate louder signals. The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system.

The DRC can apply Compression and Automatic Level Control to the signal path and replaces the ALC used by many Wolfson devices. It incorporates ‘anti-clip’ and ‘quick release’ functions for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

In some devices, the DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

DRC COMPRESSION / EXPANSION / LIMITING

The DRC supports two different compression regions, separated by a “Knee” at a specific input amplitude. In the region above the knee, the compression slope DRC_HI_COMP applies; in the region below the knee, the compression slope DRC_LO_COMP applies.

The overall DRC compression characteristic in “steady state” (i.e. where the input amplitude is near-constant) is illustrated in Figure 1.

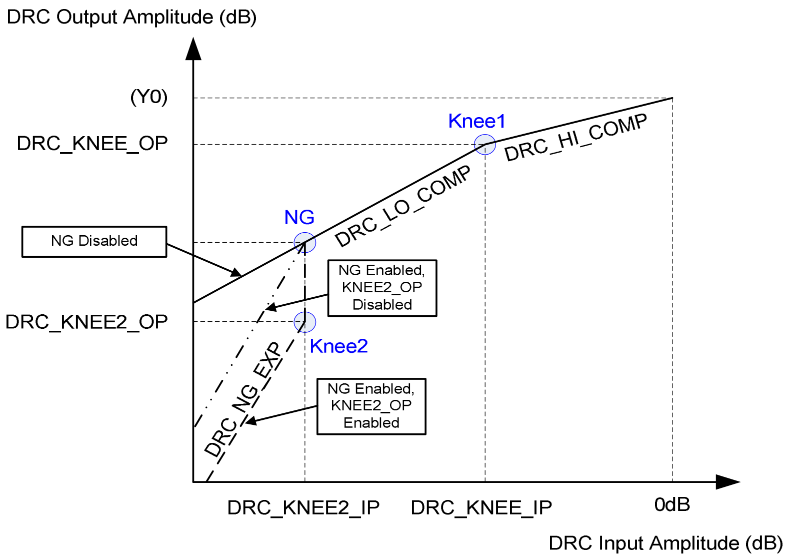


Figure 1 DRC Response Characteristic

Note that Figure 1 shows the transfer response for the DRC i.e. the output signal amplitude for a given input signal amplitude, and not the gain of the DRC. The Gain of the DRC is the difference between the input signal amplitude in dB and the output amplitude in dB

For additional attenuation of signals in the noise gate region, an additional “knee” can be defined (shown as “Knee2” in Figure 1). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response between the DRC_LO_COMP and DRC_NG_EXP regions.

The ADC HPF MUST be enabled when the DRC is used in the record path as dc offsets will cause erroneous operation.

The DRC also supports a noise gate (NG) region, where low-level input signals below the level set by DRC_KNEE2_IP are heavily attenuated. This function can be enabled or disabled according to the application requirements.

COMPRESSION

The basic DRC operation does not use the noise gate (NG) function and Knee2 has no effect as shown in Figure 2.

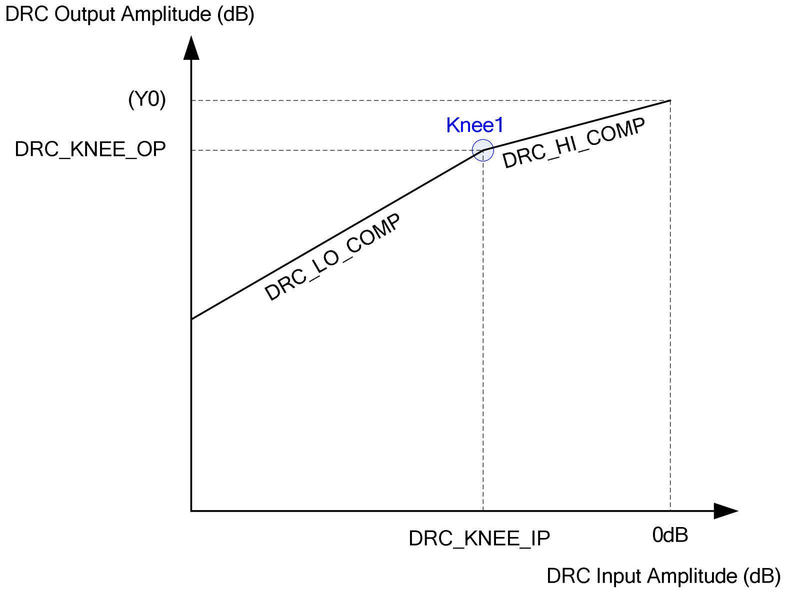


Figure 2 DRC Basic Response Characteristic

The “Knee” (Knee1) is determined by the input level DRC_KNEE_IP and DRC_KNEE_OP level. In the region above the knee, the compression slope DRC_HI_COMP applies; in the region below the knee, the compression slope DRC_LO_COMP applies.

The value Y0 is calculated from the equation below, where the Knee values are in dB and the Comp is a scalar value:

Y0 = DRC_KNEE_OP - (DRC_KNEE_IP * DRC_HI_COMP)

For example, DRC_KNEE_IP = -24dB, DRC_KNEE_OP -12dB, DRC_HI_COMP = ¼:

Y0 = -12 - (-24 * ¼) = -6dB

The compression values can be set for different DRC performance. For a compression slope of 1 there is no compression. The output signal level will change by the same amount as the input signal level changes. This is the same as having a fixed gain between the input and output signals. A compression slope of 0 results in a constant output amplitude which is the same as using an automatic level control (ALC) to maintain a constant output signal level for a varying input signal level. For compression slopes between 0 and 1, the signal level on the output signal level will change by less than change in the input signal level.

For example, if the compression slope is ¼, the change in output signal level is ¼ of the change in the input signal level. So for a 4dB change in input signal level there will be a 1dB change in output level.

The compression regions can be set independently to get the desired operation.

The registers associated with the basic DRC operation are shown in Table 2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Control 1	7	DRC_ENA	0	DRC Enable 0 = Disabled 1 = Enabled
DRC Control 4	7:2	DRC_KNEE_IP	000000	Input signal level at the Compressor ‘Knee’. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
DRC Control 5	7:3	DRC_KNEE_OP	00000	Output signal at the Compressor ‘Knee’. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
	2:0	DRC_HI_COMP	011	Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
DRC Control 7	7:5	DRC_LO_COMP	000	Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved

Table 2 DRC Registers for Basic Operation

NOISE GATE

The DRC also supports a noise gate region, where low-level input signals below the level set by DRC_KNEE2_IP are heavily attenuated. This is useful for reducing background noise during periods of silence. The attenuation is controlled by the expansion slope DRC_NG_EXP as shown in Figure 3.

The expansion slope DRC_NG_EXP can be set to rapidly reduce the output signal level when the input signal reduces. When the expansion slope is set to 1 then there is no expansion and the output signal level changes by the same as the input signal level change. If the expansion slope is set to a value greater than 1, then the output signal level changes by more than the change in input signal level.

For example, if the expansion slope is 4, then the change in output signal level is 4 times larger than the change in the input signal level. So for a 1 dB change in input signal level the output signal level will change by 4dB.

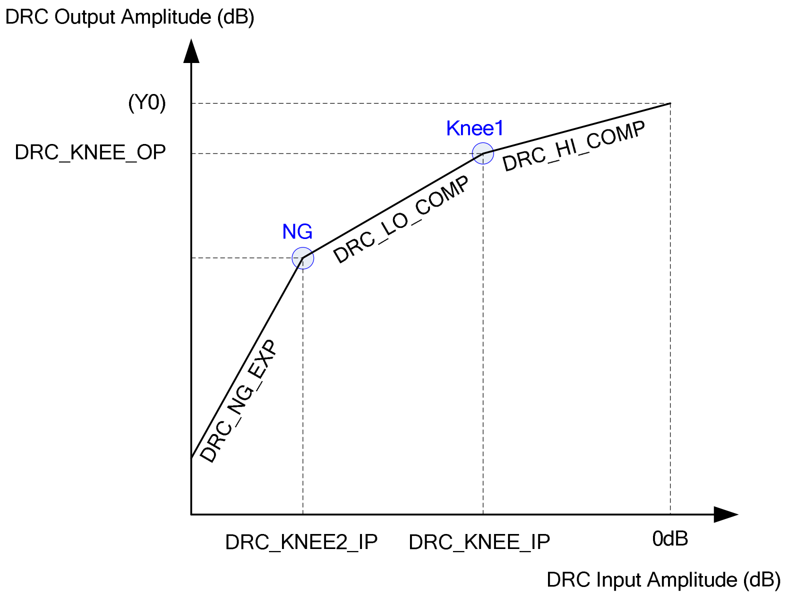


Figure 3 DRC Response Characteristic with Noise Gate

The input signal level where the NG takes affect is set by DRC_KNEE2_IP.

The additional registers associated with the NG function are shown in Table 3. Note that the DRC should be set for basic operation as described in the previous section.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Control 1	8	DRC_NG_ENA	0	DRC Noise Gate Enable 0 = Disabled 1 = Enabled
DRC Control 4	12:8	DRC_KNEE2_IP	000000	Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.
DRC Control 7	9:8	DRC_NG_EXP	00	Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8

Table 3 DRC Registers for Noise Gate Operation

NOISE GATE WITH KNEE2

For additional attenuation of output signal levels in the noise gate region, an additional "knee" can be defined, shown as "Knee2" in Figure 4. When this knee is enabled (DRC_KNEE2_OP_ENA=1), this introduces an infinitely steep drop-off in the DRC response between the DRC_LO_COMP and DRC_NG_EXP regions as shown in Figure 4.

For example, if DRC_KNEE2_IP is set to -40dB and DRC_KNEE2_OP is set to -30dB, when the input signal level reduces to -40dB the output signal level will drop to -30dB. So if the output signal level is -20dB when the input signal is just above DRC_KNEE2_IP (-40dB), when the input signal drops to -40dB the output signal will drop to -30dB.

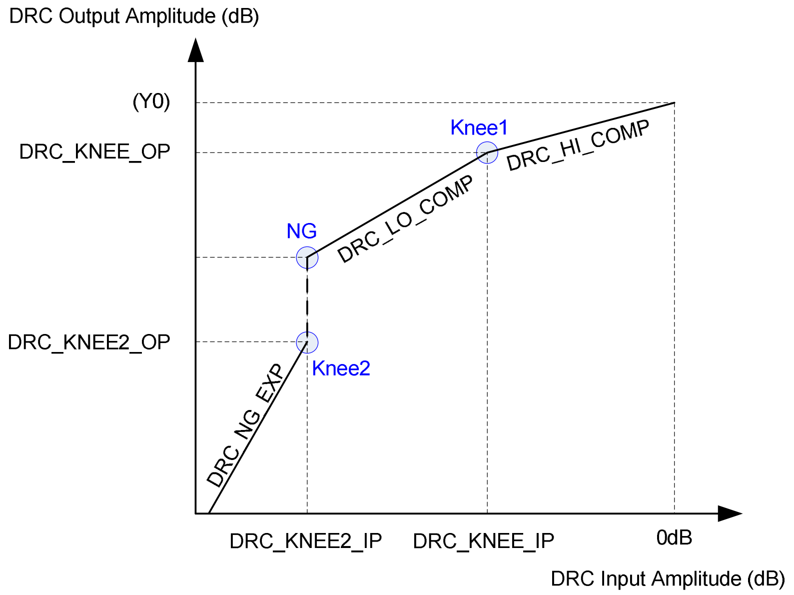


Figure 4 DRC Response Characteristic with NG and Knee2

The additional registers associated with the Knee2 function are shown in Table 4. Note that the DRC should be set for NG operation as described in the previous section.

Setting DRC_KNEE2_OP_ENA to 1 when DRC_NG_ENA=0 will have no effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Control 5	13	DRC_KNEE2_OP_ENA	0	DRC_KNEE2_OP Enable 0 = Disabled 1 = Enabled
	12:8	DRC_KNEE2_OP	00000	Output signal at the Noise Gate threshold ‘Knee2’. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.

Table 4 DRC Registers for Noise Gate with Knee2 Operation

GAIN LIMITS

The minimum and maximum gain applied by the DRC is set by registers DRC_MINGAIN, DRC_MAXGAIN and DRC_NG_MINGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 1 to Figure 4. If the range between maximum and minimum gain is reduced, as shown in Figure 5, then the perceived loudness/intelligibility generally improves, at the expense of reduced dynamic range.

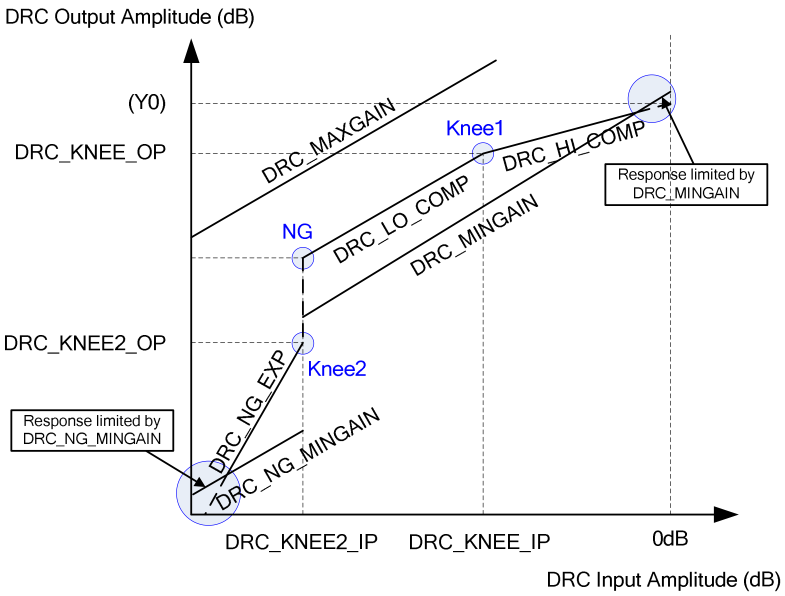


Figure 5 DRC Response Characteristic with Max and Min Gain Limits

The minimum gain in the Compression regions of the DRC response is set by DRC_MINGAIN. The minimum gain in the Noise Gate region is set by DRC_NG_MINGAIN. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by DRC_MAXGAIN prevents quiet signals (or silence) from being excessively amplified. The registers associated with the gain limits are shown in Table 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Control 2	12:9	DRC_NG_MINGAIN [3:0]	0110	Minimum gain the DRC can use to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	4:2	DRC_MINGAIN [2:0]	001	Minimum gain the DRC can use to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	DRC_MAXGAIN [1:0]	01	Maximum gain the DRC can use to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB

Table 5 DRC Gain Limits

GAIN READBACK

The gain applied by the DRC can be read from the DRC_GAIN register. This is a 16-bit, fixed-point value, which expresses the DRC gain as a voltage multiplier.

DRC_GAIN is coded as a fixed-point quantity, with an MSB weighting of 64. The first 7 bits represent the integer portion; the remaining bits represent the fractional portion. If desired, the value of this field may be interpreted by treating DRC_GAIN as an integer value, and dividing the result by 512, as illustrated in the following examples:

DRC_GAIN = 05D4 (hex) = 1380 (decimal)

Divide by 512 gives 2.914 voltage gain, or 4.645dB

DRC_GAIN = 0100 (hex) = 256 (decimal)

Divide by 512 gives 0.5 voltage gain, or -3.01dB

The DRC_GAIN register is defined in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Status	15:0	DRC_GAIN [15:0]		DRC Gain value. This is the DRC gain, expressed as a voltage multiplier. Fixed point coding, MSB = 64. The first 7 bits are the integer portion; the remaining bits are the fractional part.

Table 6 DRC Gain Readback

DYNAMIC CHARACTERISTICS

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. If the output amplitude were to follow the compression characteristics instantaneously, the waveform shape would be altered and distortion would be produced.

Note that the DRC responds to the peak signal amplitude over a period of time.

When the DRC is operating as a compressor, the gain reduces when the input signal increases. The DRC utilises attack and decay rates to control the dynamic behaviour of the gain. When the gain reduces, the DRC_ATK rate controls the rate of decrease in gain. When the gain increases due to a decrease in signal level, the DRC_DCY rate controls the rate of increase in gain as shown in Figure 6.

Note that the actual levels that the DRC settles to depend on the input signal and the DRC response.

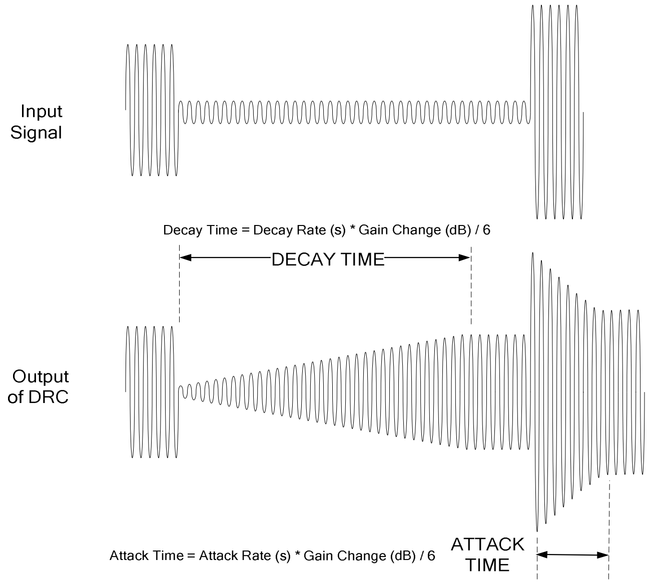


Figure 6 Attack and Decay Rates

Generally a fast attack rate is preferred to allow the system to respond quickly to transients to prevent clipping, and a slow decay rate is preferred to prevent the gain fluctuating in the presence of high amplitude low-frequency signals. These register fields are described in Table 7.

Note that the register defaults are suitable for general purpose microphone use. For high quality music recording it is recommended that a longer decay rate is used.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Control 3	7:4	DRC_ATK [3:0]	0100	Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved
	3:0	DRC_DCY [3:0]	0010	Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved

Table 7 DRC Attack and Decay Rates

The DRC_ATK and DRC_DCY rates are specified in seconds/6dB step. This means that the time for the output signal to recover from a change in the input signal level depends on the size of the change in input signal amplitude.

The DRC_ATK and DRC_DCY rates also increase due to the DRC_HI_COMP setting. The output rate is given by

Output DRC_ATK = DRC_ATK (Datasheet Value) / (1-R0)

where R0 is the value of the DRC_HI_COMP register.

For example, if the input signal level increases by 15dB with the DRC_ATK rate set at 1.45ms, sample frequency of 32kHz, and the DRC_HI_COMP is set to ½, the time for the output signal to recover from the input signal level change will be 15dB / 6dB * 1.45ms = 3.625ms. The DRC_HI_COMP setting is ½ so allowing for this gives an estimated Attack time of 3.625ms / (1-1/2) = 7.25ms.

Due to the non-linear behaviour of the peak detector the output attack rate is also affected by the frequency of the input signal. This is not predictable and can only be estimated at up to three times the calculated value.

ANTI-CLIP CONTROL

When a small signal is applied to the DRC, a high gain is set. If this is followed by a large signal, the gain must reduce quickly to prevent the output signal clipping, as shown in Figure 7.

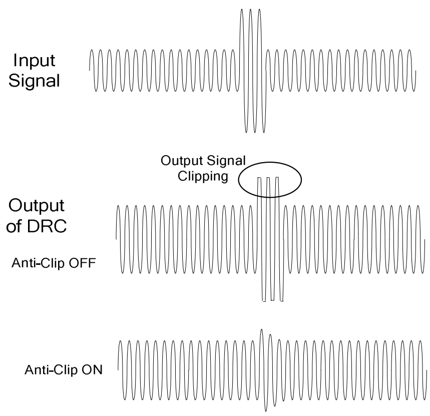


Figure 7 Anti-Clip Control

The DRC includes an Anti-Clip feature to reduce signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is minimised by switching to a fast attack rate when required.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Control 1	1	DRC_ANTICLIP	1	DRC Anti-clip Enable 0 = Disabled 1 = Enabled

Table 8 DRC Anti-Clip Control

The Anti-Clip feature will not guarantee that the signal does not clip in all conditions but will reduce the effect of any clipping that does occur.

The Anti-Clip feature is enabled using the DRC_ANTICLIP bit (see Table 8). The feed-forward processing increases the latency in the input signal path.

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

QUICK-RELEASE CONTROL

When a short transient signal is applied to the DRC, it will normally attack (reduce the gain) quickly, then decay (increase the gain) slowly, as shown in Figure 8. As a consequence, audible drop-outs in the output signal can be detected.

The DRC includes a Quick-Release (QR) feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer rates of DRC_DCY.

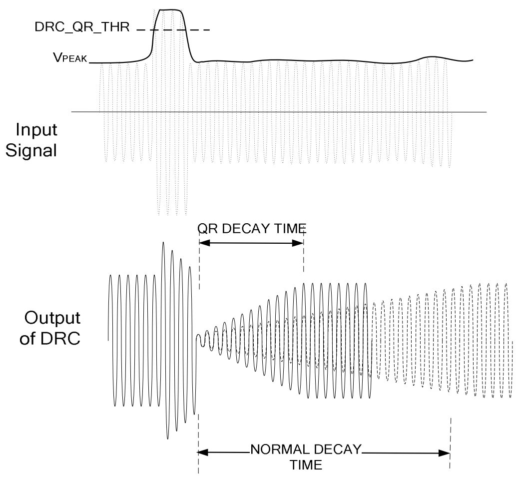


Figure 8 Quick Release Control

The QR feature is enabled by setting the DRC_QR bit. When this bit is enabled, the DRC monitors the input signal. If a transient peak is detected it may not be related to the intended source signal. If the transient exceeds the level set by DRC_QR_THR, then the normal decay rate DRC_DCY is ignored and a faster decay rate DRC_QR_DCY is used instead.

A separate Quick-Release feature is provided for the Noise Gate response. In the case of the signal level rising after a period of silence, the Noise Gate Quick-Release enables the DRC to transition out of the noise gate attenuation region at a faster rate than the normal decay rate. The Noise Gate Quick-Release feature is enabled by setting the DRC_NG_QR bit.

The DRC Quick-Release control bits are described in Table 9.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
DRC Control 1	5	DRC_NG_QR	0	DRC Noise Gate quick-release Enable 0 = Disabled 1 = Enabled
	2	DRC_QR	1	DRC Quick-release Enable 0 = Disabled 1 = Enabled
DRC Control 6	3:2	DRC_QR_THR [1:0]	00	DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	1:0	DRC_QR_DCY [1:0]	00	DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved

Table 9 DRC Quick-Release Control

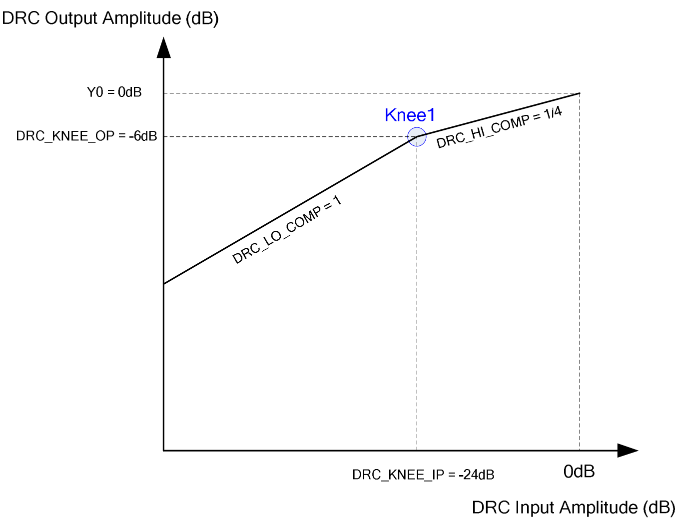
APPLICATIONS

This section discusses some examples of using the DRC in different applications.

PEAK LIMITER

In a limiter, the signal level is unchanged for amplitudes below the knee, but sharply reduced for amplitudes above the knee. Normally the knee will be at a high amplitude e.g. around -6dB, so that the majority of the dynamic range is unchanged.

For example, if a microphone is “distant” from the sound source the output signal from the microphone may be around -54dBV. If the signal is amplified by the microphone PGA (typically +30dB) the input level to the ADC is -24dBV. With the limiter configuration below, the signal amplitude will be boosted digitally (by +18dB) to -6dB. When the sound source is 1cm from the microphone, the output signal from the microphone will be higher and may be around -34dBV. After amplification (+30dB) the signal level to the ADC is -4dBV. If the same amount of gain were applied digitally (+18dB) the signal would clip. By applying less gain the limiter configuration below will ensure that the signal does not clip (in the steady state).



PARAMETER	VALUE
DRC_KNEE_IP	-24
DRC_KNEE_OP	-6
DRC_HI_COMP	1/4
DRC_LO_COMP	1

ALC

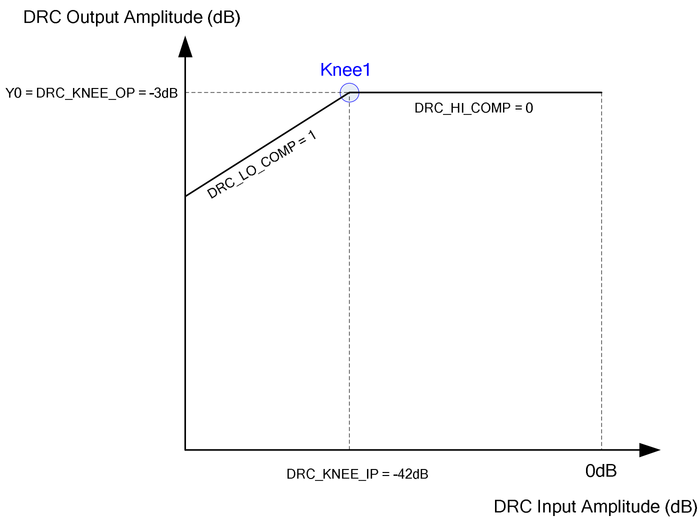
An ALC is used to equalise volume settings so that quiet small-amplitude signals are boosted to achieve the same amplitude as high-amplitude signals.

A typical application for this is Digital Still-Cameras (DSC) , for record applications, where the source that is being recorded is a variable distance from the microphone, but must be recorded at more or less the same output level to maintain intelligibility of the signal. Another key application is line-level recording, where different input sources have different signal levels, but should be equalised to the same level automatically.

TRADITIONAL ALC

A typical traditional ALC characteristic is shown below. A compression slope of zero (constant amplitude) is used for signals above the knee, and a slope of 1 (constant gain) is used below the knee. The latter limits the gain for very small signals to reduce the amplification of noise from the input source. One of the disadvantages of an ALC is that a very high gain can be produced even for relatively low signal amplitudes. Side effects such as gain-pumping can become very apparent with this gain characteristic, making the ALC unsuitable for music recording, unless very long decay times are used.

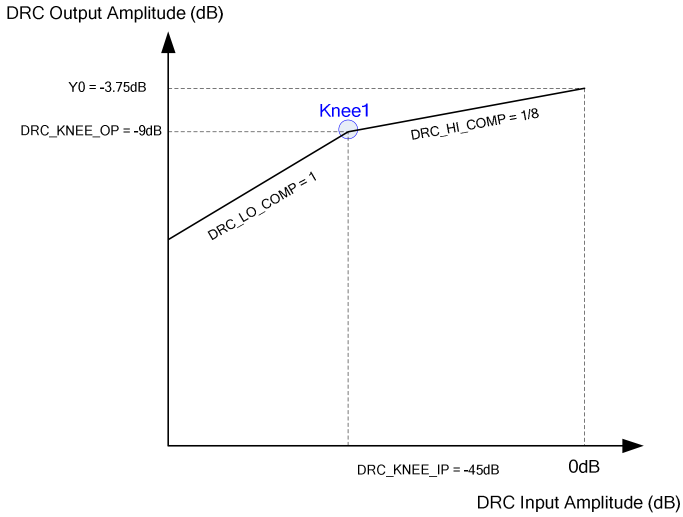
Note that in the example below a threshold of -3dB is used to allow for some overshoot of the input signal which allows the ALC some time to respond before clipping occurs.



PARAMETER	VALUE
DRC_KNEE_IP	-42
DRC_KNEE_OP	-3
DRC_HI_COMP	0
DRC_LO_COMP	1

‘SOFT’ ALC

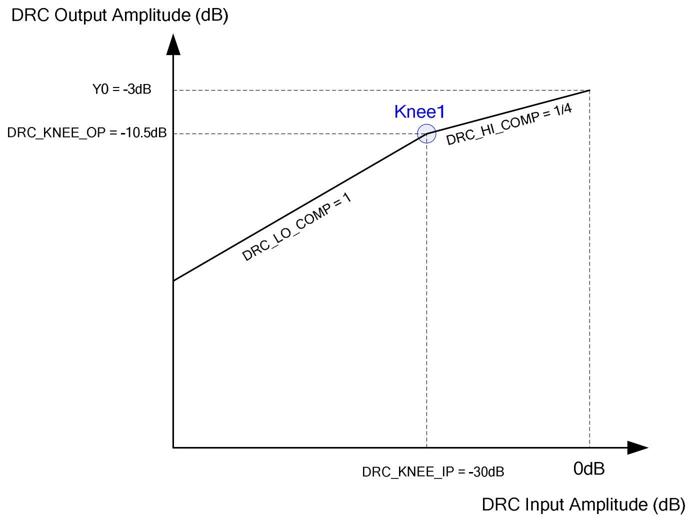
A ‘soft’ ALC is used in applications where a gentler ALC characteristic is required, for example where both speech and music recording is required without reconfiguring compressor parameters. An additional advantage of this configuration is that some of the dynamic range properties of the original signal is preserved, i.e. the loudness of the signal is still proportional to the distance from the microphone (although the dynamic range is still squashed), which makes recorded conversation more natural.



PARAMETER	VALUE
DRC_KNEE_IP	-45
DRC_KNEE_OP	-9
DRC_HI_COMP	1/8
DRC_LO_COMP	1

MUSIC ALC

This uses even gentler compression characteristics and uses a higher knee threshold to limit the gain to around 20dB.



PARAMETER	VALUE
DRC_KNEE_IP	-30
DRC_KNEE_OP	-10.5
DRC_HI_COMP	1/4
DRC_LO_COMP	1

SUMMARY

The DRC used in the latest Wolfson CODECs can be enabled in the digital playback or digital record path of the CODEC, depending upon the selected DSP mode. The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system.

The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' functions for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

The operation of the DRC used has been discussed and the registers associated with the DRC functions have been detailed. There are numerous possible settings that can be implemented with the DRC and a few of the main application areas have been highlighted.

APPLICATION SUPPORT

If you require more information or require technical support please contact Wolfson Microelectronics Applications group through the following channels:

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