

## CS4525 2.1 Layout Reference and Guidelines

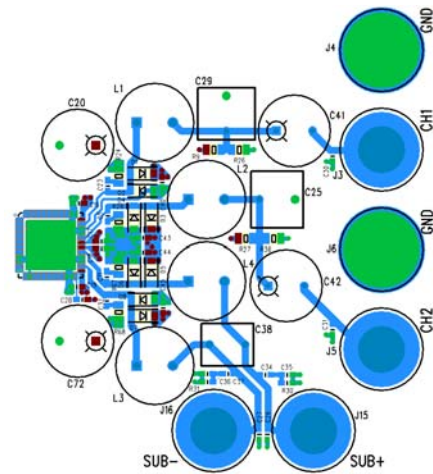
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Class D amplifiers have several advantages over traditional Class A/B amplifiers. These include higher operating efficiencies, less thermal dissipation, and smaller form factors. However, in order to realize these advantages some changes are required relative to a traditional Class A/B amplifier board design. The board design changes are not difficult to implement, but are less familiar to most designers than techniques used for Class A/B amplifiers. Careful consideration to the circuit board layout should be taken up front in order to ensure a successful design.

This application note addresses the layout guidelines and provides layout references specific to the Cirrus Logic CS4525. The CRD4525-Q21 board is used as a layout example for a 2.1 speaker output configuration of the CS4525. This board should be used as a reference for all 2.1 speaker output configuration designs using the CS4525. For reference, full schematics and layout diagrams of the CRD4525-Q21 are provided in [Section 4](#).

This application note is divided into 3 major sections. [Section 1](#) is an overview of the high level board design subjects and how to get started. [Section 2](#) and [Section 3](#) focus on the component placement and board layout specific to a 3 channel, 2.1 output configuration, full-bridge board design, using the CRD4525-Q21 board as a reference. Component placement is discussed separately from layout and routing.

When designing the layout of a board without a reference the process normally begins with determining how everything will piece together during component placement. Most of the board is defined in this stage. Typically, only minor changes in placement are made once placement is complete unless a specific change is found to be required during layout. This document follows the same basic process flow. The high level decisions are made first. Component placement is then selected. The layout and routing complete the major design stages.



**Figure 1. CRD4525-Q21  
Key Component Layout**

## 1. LAYOUT CONSIDERATIONS OVERVIEW

### 1.1 Board Layers & Stack Up

When starting, the first design choice to be made with a Class D amplifier is whether to use a 2 or 4 layer printed circuit board. While attractive from a production cost viewpoint, 2 layer boards rarely present the anticipated production cost savings and invariably increase the time and cost of the product development cycle. There are many more electrical considerations that must be taken when using a 2 layer board with regards to radiated and conducted EMI, creating long return paths, and other related performance issues.

Unless the engineer is familiar with developing and debugging Class D amplifiers on a 2 layer board it is suggested that the amplifier be developed on a 4 layer board. This approach has been shown to produce consistent and reliable results when following the basic design guidelines within this application note. Also, it should be considered that a complete system design using the CS4525 typically consists of a 4 layer board for reasons not primarily driven by the CS4525.

As follows, the information contained in this document is focused on a 4 layer board design implementation. The CS4525 reference board design referred to in this document is based on a 4 layer design. The stack up of the board is composed of a top layer of ground and signal traces, a second layer of ground only, a third layer containing the CS4525's two power supplies, and a fourth layer of ground and a few signal traces.

This is the suggested stack up for a 4 layer board. It is highly recommended that both the internal and external layers of the board use at least 1 oz. copper for improved thermal dissipation and reduced electrical inductance.

**Layer 1:** Components, signals, and the remaining areas filled with ground.

When using a 4 layer stackup the top layer is referred to as layer 1. This layer should contain a bulk of the signal paths, all of the components, and any remaining areas should be filled with ground. Most of the information in this document is focused on component placement, layout, and routing of layer 1. More information on the ground fill can be found in [Section 3.10 on page 16](#).

**Layer 2:** Ground plane.

Layer 2 should be used as a solid ground plane. The ground plane should be located on layer 2 to allow for a consistent ground connection from components placed on layer 1, and to allow for layer 1 signals to electrically perform as microstrips, with the image path directly under the signal trace. No signals should be routed on layer 2 to provide a solid return path. More information can be found in [Section 3.8 on page 15](#).

**Layer 3:** VP power plane and VD power plane.

Layer 3 should be used as the power distribution plane. The two boards used as references in this document contain 2 power supply domains. The low power, 3.3 V power supply is referred to as VD. The higher power, 18 V power supply is referred to as VP. Layer 3 should be split between VD and VP. No signals should be routed on layer 3.

Most of the content in this document is focused on components connected to and supplied by the VP power supply. More information on partitioning layer 3 between VD and VP can be found in [Section 3.9 on page 15](#).

**Layer 4:** Signals and GND fill.

Layer 4 should be used to fit any remaining signals onto the board that could not be routed on layer 1. The majority of this layer should be filled with ground, especially in the area surrounding the CS4525. This will allow better thermal dissipation, improved board decoupling capacitance, and a more consistent ground return. More information on layer 4 can be found in [Section 3.10 on page 16](#).

## 1.2 CRD4525-Q21 Board Reuse

In order to ensure maximum flexibility of the CRD4525-Q21 board, binding post terminals, connectors to the CDB45DB1 control board, and a socketed crystal oscillator socket are used. Although this increases end user flexibility with these boards, it also artificially increases the size of the board. It should be noted that the CRD4525-Q21 board is larger than the footprint that would be required with an integrated design. Some sizing and layout compromises have been made in order to retain the most general functionality of this board.

With the exception of the components listed above the CRD4525-Q21 board layout has been developed so that a designer may simply copy and paste a majority of the layout into their design with minimal effort up front.

The CRD4525-Q21 reference design has a break out board attached to the back side of the amplifier board. The breakout board is separated at assembly, and for purposes of this document will not be discussed. The existence of the breakout board is noted here only to minimize confusion when referring to the CRD4525-Q21 PCB layout files or gerber files.

### 1.3 Definitions and Terms

**CDB45DB1** - The control and audio input board which can be used to connect to the CRD4525-Q21 board. This board houses contains analog inputs, a SPDIF receiver, and allows for complete control of the CRD4525-Q21 board using a USB connection to a PC and the Cirrus Logic Flex GUI software.

**GND** - The ground that resides on the printed circuit board.

**PGND** - The CS4525 ground pins that are connected to the P-FET / N-FET audio output driver pair.

**Switching outputs** - Refers to pins 26, 29, 32, and 35 of the CS4525 or the equivalent node on the board between the CS4525 and the inductor on the LC filter.

**OUT1, OUT2, OUT3, OUT4** - Refers to a specific switching output channel of the CS4525 and its signal path all the way to the binding post terminals: OUT1 = pin35, OUT2 = pin32, OUT3 = pin29, OUT4 = pin26.

**Speaker outputs** - Refers to the OUT1 to OUT4 signals between the inductors on the LC filter and the speaker output connectors (or binding posts on the CRD4525 boards).

**Speaker output connectors** - Refers to the physical connector that resides on one of the speaker outputs.

**Backend components** - This includes any resistors, capacitors, inductors, or diodes that are a part of the connections between the CS4525's switching outputs and the board's speaker outputs.

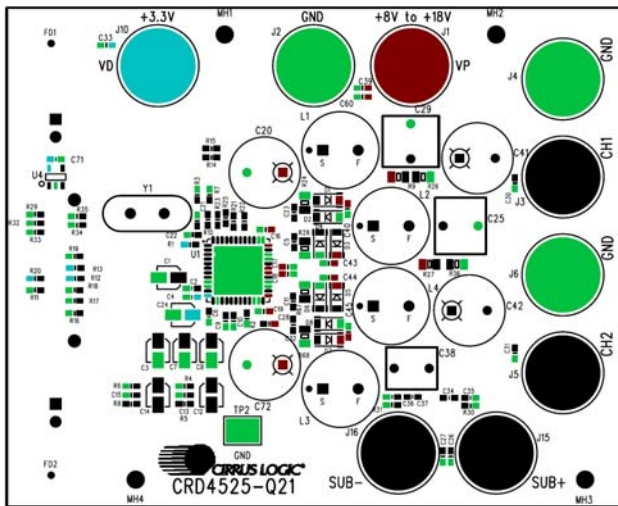
**Key components** - These components have been identified as very important with regards to the placement and layout routing for the CS4525 Class D amplifier system.

**Anti-peaking circuits** - This RC circuit is used to dampen the frequency response peak of the full-bridge LC circuit when there is no speaker load on the outputs.

**EMI capacitors** - Small value, shunt capacitors placed near the speaker output connectors in order to attenuate unwanted high frequency noise from radiating off the board onto the speaker cables.

## 2. CRD4525-Q21 FLOOR PLAN & COMPONENT PLACEMENT

The board sections which require the most attention to detail when determining a floor plan and component placement are the areas connected to the VP power domain. The intrinsic design of a Class-D amplifier dictates that the voltage supply providing power to the switching output FETs will require the most attention. Proper board design will reduce the potential for inducing ringing on the power supply, creating common mode noise, producing undesirable radiated EMI emissions, and producing reduced output performance. The key components for the VP power domain consists of decoupling capacitors, the RC snubber network, Schottky protection diodes, the low pass LC filter, optional anti-peaking circuits, and shunt EMI capacitors.



**Figure 2. CRD4525-Q21 Component Placement**

The floor plan and placement flow in this document focuses on key components in the VP power domain, starting with items closest to the CS4525 and then working outward. Keep in mind that the CRD4525-Q21 has been designed with general purpose use and flexibility in mind. Areas and non-key components not residing on the VP power domain (such as the low power digital and analog I/O on the VD power domain) may vary based on application and sizing needs. These connections are relatively straightforward and may be handled in a similar manner as with a Class A/B amplifier or other audio solution.

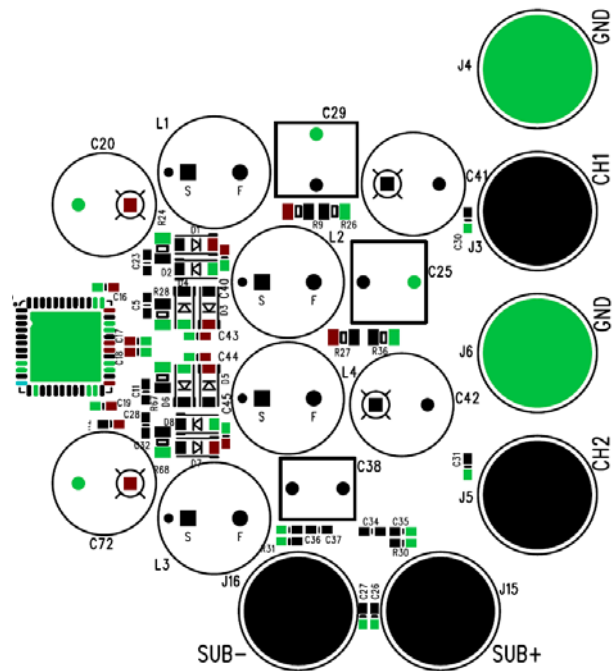
Figure 2 shows the component placement for the entire CRD4525-Q21 board. With the exception of a board mating socket on the bottom of the board, all components are placed and routed on the top layer. For most applications it is not necessary to populate both sides of the board. A small and efficient amplifier design can be developed using only single sided component population.

Double sided component population can potentially be used to reduce the total amplifier footprint. However, unless the end system already requires two sided board population, this is done at additional cost and is outside of the scope of this document.

Figure 3 shows the key components and their locations for a proper layout with the CS4525-Q21. The binding post terminals are left on this example to show their relative output locations. Most typical applications will use much smaller speaker output connectors and will not require as large of a footprint.

Much of the component placement between the CS4525 and LC filter inductors is symmetric to the center of the CS4525. However, a 2.1 speaker output configuration requires different components for the 2 half-bridge and 1 full-bridge output. With 3 speaker outputs there is also a greater possibility of needing to rearrange some of the larger components on the LC filter placement in order to keep the total amplifier design small.

Components that are focused on in the following sections will be highlighted in red. The components which have already been placed will be grayed out. The CS4525 will be left with its original placement color scheme.



**Figure 3. CRD4525-Q21 Key Component Placement**

## 2.1 Decoupling Capacitor Placement

### 2.1.1 Small Value Decoupling Capacitors

There are 4 P-FET / N-FET bridges on the CS4525 that produce the switching outputs (OUT1 - OUT4). With any FET switching event, current is drawn from the power supply and, without adequate bypassing, power supply noise can be generated. The best way to mitigate this high frequency power supply noise is with decoupling capacitors. In order to reduce the total high frequency loop distance, **the decoupling capacitors should be as close to the CS4525 as possible**, shown in [Figure 4](#). On the top side (pins 36 - 38) and bottom side (pins 22 - 25) of the CS4525 this is straightforward. During routing, vias will be placed on the outside of each of the two small decoupling caps (C16 and C19). This will keep the loop of the high frequency, electrical noise generated by a switching event short and efficient.

When placing C19, make sure to align it so that pin 24 is centered between the GND and VP pads of the capacitor. This will allow for routing of the ramp capacitor (C28) that supports the half-bridge pop suppression.

The CS4525 requires the use of the ramp capacitor (C28) to minimize any turn-on and turn-off transients with half-bridge outputs. Place the ramp capacitor pad of C28 so that a straight line can be drawn between pin 24 on the CS4525, through the center of C19, and to the center of the C28 pad. The VP pad of C28 should be orientated towards the backend components.

With the center 2 FET pairs (OUT2 and OUT3) more care is required during the layout phase in order to not interfere with the switching outputs during routing. For now, the VP side of the C18 should reside in front of pin 30, and the VP side of C17 should reside in front of pin 31. The GND side of both capacitors should be facing away from the CS4525 as shown in [Figure 4](#).

### 2.1.2 Electrolytic Capacitors

The 2 radial, **through-hole, electrolytic, bulk capacitors are placed adjacent to the CS4525 with VP and GND at an approximately equal distance from the CS4525**. The VP pole of the capacitor should be facing towards where the backend components will eventually reside. Through-hole bulk capacitors are preferred if possible. They will typically allow for a less inductive and more consistent connection to the internal GND and power supply layers. This will maximize their effectiveness.

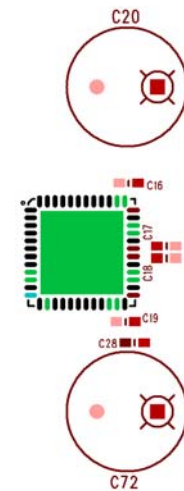


Figure 4. Capacitor Placement

## 2.2 Snubber Placement

The first components to be placed for the full-bridge switching outputs should be the single ended RC snubbers. The snubbers are used to reduce the ringing on the rising and falling edges of the switching PWM waveforms. **Figure 5 shows the location and orientation of the RC snubbers.**

The input side of C5, C11, C23, and C32 should be placed so that during routing their landings will reside directly on top of the OUT1 - OUT4 pre-LC filter, switching output traces. The other pad of the 4 snubber 0603 COG capacitors should be adjacent to the 0805 resistor pads (R24, R28, R67 and R68) in order to keep the snubber footprint small and compact. **Improper placement of the snubbers can reduce their effectiveness and ability to reduce ringing and potentially lead to EMI problems.**

Keep in mind that the CRD4525-Q21 demonstrates 3 output channels. This requires some of the layout to be not completely symmetric. The first example of this is when placing the snubber capacitors and resistors. C5 and C23 require slightly more distance between them than C11 and C32 do. There will eventually be a small isolating ground trace that is run between OUT1 and OUT2 to help prevent crosstalk between the two half-bridge outputs, and is discussed further in [Section 3.3](#).

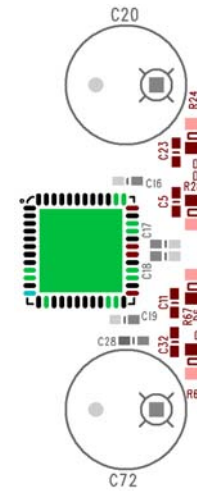


Figure 5. Snubber Placement

## 2.3 Protection Diode Placement

A pair of Schottky diodes are required on each of the 4 switching outputs. **These diodes (D1 - D8) should be placed immediately after the RC snubber networks.** The closer to the CS4525 the diode pairs are placed, the more effective they will be. If these diodes are placed too far from the CS4525 they may not be able to protect the switching outputs properly and risk damage to the device. A high side (OUTx to VP) and low side (OUTx to GND) Schottky protection diode are used for each switching output (OUT1 - OUT4). The input pads of the high and low side diode should be lined up, as shown in [Figure 6](#), so that they will end up residing on top of the traces similar to the capacitor pads on the RC snubbers during layout and routing.

The low side diode should be placed closest to the snubber. This will allow the GND connections for the snubber and low side diodes to be next to each other. The high side diode should then be placed next to the low side diodes farther away from the CS4525.

**The diode pairs connected to OUT1 and OUT4 should be rotated 90 degrees to accommodate the routing** required for the 3 speaker outputs as shown on the CRD4525-Q21. Due to the filtering requirements for the half-bridge outputs and in order to keep the total footprint small, OUT1 and OUT4 signal paths are run vertically away from the diodes, instead of horizontally as with OUT2 and OUT3. More details on this are provided in [Section 3.3](#)

The diodes are used to protect the CS4525 from voltage overshoot and undershoot of the switching waveform. It is recommended that RB160M-30 diodes or an equivalent be used. If the electrical characteristics of the diode are incorrect, they may not be effective in reducing overshoot or undershoot which could cause damage to the CS4525.

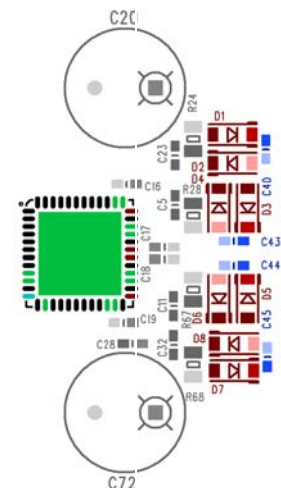


Figure 6. Diode Placement

**C40, C43, C44, and C45 (shown in [Figure 6](#)) should be placed so that they are adjacent to each protection diode pair's GND and VP connections.** These diode pair capacitors are used to reduce ringing that can be created by the protection diodes. The protection diodes can switch on and off very quickly after

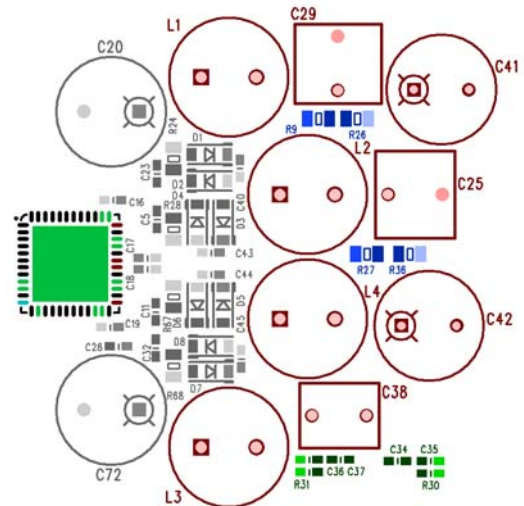
a rising or falling edge of the CS4525's outputs. This can be observed as ringing on the power supply and speaker outputs.

Population of these 4 capacitors is optional. However, it is recommended that the pads and connections be put in place. Each PCB design has different characteristics, and if it is determined that they are not necessary, they can simply be left unpopulated.

## 2.4 Low Pass LC Filter Placement

A 2.1 speaker output configuration using the CS4525 contains two half-bridge output filters and one full-bridge output filter. In order to keep the total amplifier design small, there will be differences in LC filter component placement for each output.

**The inductors should be placed as close as possible to the Schottky diodes** and each other. L1 and L3 are placed close to the bulk capacitors. This should create an approximately straight line between the pads of D1, D2, D7, D8, and the inputs of L1 and L3. L2 and L4 are lined up with each other immediately after the Schottky diodes. This placement will allow the OUT1 - OUT4 signal traces to be kept approximately the same distance from the CS4525 to the inductors of the LC filter, and for the high frequency switching output nodes to be kept small as shown in [Figure 7](#).



**Figure 7. Low Pass LC Filter Placement**

Because the inductors are staggered to keep the total footprint small, the full-bridge outputs will not be able to be run differentially throughout the signal path. C38 should still be placed as close to L3 and L4 as possible. This placement and orientation shown in [Figure 7](#) will assist in keeping the layout traces a similar length and will allow them to be brought together as a differential pair again before reaching the output terminal.

The CRD4525-Q21 is used as an example of how two different half-bridge LC filter placement techniques can produce the desired performance results. In this example, where the speaker output terminals reside is taken into consideration when placing C25, C29, C41, and C42. This is illustrated with the placement locations of the binding post terminals for OUT1 / CH1 and OUT2 / CH2 on the CRD4525-Q21 board, shown in [Figure 3](#). The output terminal for CH1 resides close to C41. This allows L1, C29, and C41 to be lined up, keeping the component footprint and signal path short. The resulting connections will form a straight line. Because large binding posts are used on the CRD4525-Q21, the output terminal for CH2 is located further down the board. To conserve board space and reduce total trace length a straight line placement is not used. C25 and C42 are placed next to the inductors (L2 and L4). The output side of C42 is in the vicinity of the CH2 output terminal.

The flexibility with the placement scheme of the half-bridge outputs, after passing through the inductors, is due to their single ended nature. The half-bridge outputs require no differential routing and use GND as a return path. Additionally, as with a full bridge output, most of the high frequency energy is attenuated after passing through the inductor. **The key factor allowing this flexibility is that the metal film capacitors are kept (C25 and C29) close to the output of the inductors (L1 and L2).**

## 2.5 Anti-Peaking & Pop Suppression Circuits

### 2.5.1 Full Bridge Anti-Peaking Circuit Placement

The anti-peaking RC circuits (R31, C36, C37, C34, C35, and R30) are put in place on the full-bridge outputs of the CRD4525-Q21 to prevent LC filter oscillation when the outputs are left unloaded. In an application where an output load is guaranteed these filters are not required, and they may be removed from the design. **The anti-peaking circuits should be placed adjacent to or slightly after the film capacitor on the LC filter, highlighted green in Figure 7.** However, if the space available for the layout dictates, the anti-peaking circuits may be moved closer to the speaker outputs. If they are not adjacent to the film capacitors on the LC filter (C29 and C38), it is recommended that they are both placed a similar distance from the LC filter for purposes of electrical consistency.

The half-bridge outputs do not require anti-peaking circuits under any loading condition.

### 2.5.2 Half-Bridge Anti-Pop Circuit Placement

The half-bridge anti-pop circuit is required to slowly bring up the charge of the DC blocking capacitor to  $VP/2$  when operating at voltages above 15V. These resistor dividers (R9, R26, R27, and R36) will reduce the power up transients when enabling the switching outputs of the CS4525 while operating in a half-bridge configuration.

**The half-bridge anti-pop circuits are required to be placed between the inductor of the LC filter and the DC blocking capacitor.** The exact location on this electrical node is not critical. However, try to place them in a location that is in line or close to being in line with the expected output signal trace. Do not place them in a location that will require branching off long distances to connect these resistors. Examples of how to place these resistors are shown in Figure 7, highlighted in blue.

## 2.6 EMI Capacitor Placement

Small shunt capacitors are put in place in order to attenuate any remaining EMI energy on the speaker outputs. **These capacitors should be placed just before the speaker outputs.**

It is understood that with certain designs there could be some distance between the CS4525's outputs and the speaker output terminals. Keeping the EMI capacitors close to the speaker output terminals will allow for the attenuation of any additional noise picked up on the board along the way to the speaker outputs.

Figure 8 shows the placement of the 4 EMI capacitors used on the CRD4525-Q21 board. The 2 EMI capacitors are placed between the large binding post terminals on the full-bridge output (SUB+ and SUB-). The half-bridge outputs (CH1 and CH2) each require a single EMI capacitor placed in line with the expected signal path and before the terminal. The other terminal for each half-bridge output is GND, and therefore does not require a second EMI capacitor.

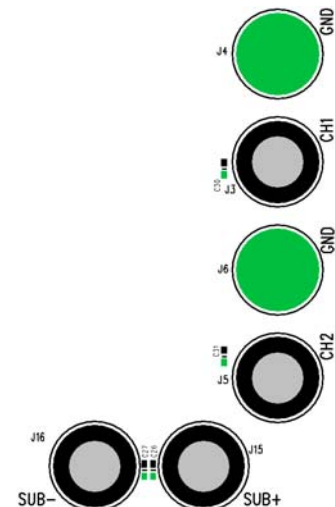


Figure 8. EMI Capacitor Placement

### 3. CRD4525-Q21 FULL-BRIDGE LAYOUT & ROUTING

With the components being placed on the top layer, most of the CRD4525-Q21 layout and routing discussion is focused on layer 1.

Placing most of the signal traces and components on top will help keep costs low, simplify the board design, allow for a compact design, and improve thermal performance on the bottom side of the board.

Figure 9 illustrates the component placement and routing of the CS4525 and key components on the CRD4525-Q21.

There are additional components and signals required by the CS4525 to operate properly. However, they are not shown to avoid any confusion on what sections and signals of the layout require the most attention to detail.

Refer to the CS4525 data sheet for more information on the other system components and connections.

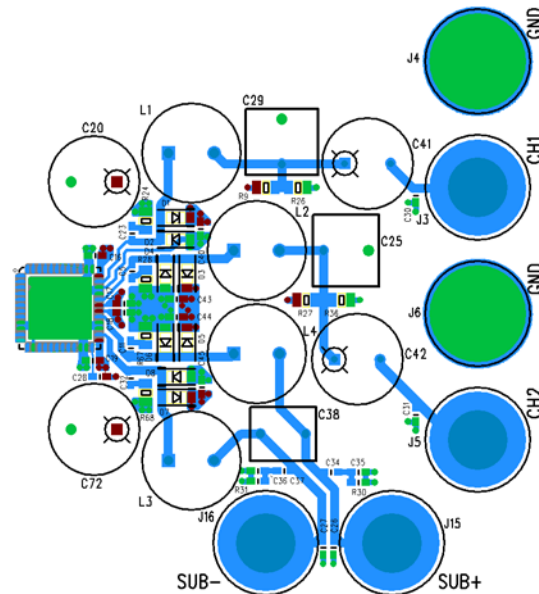


Figure 9. CRD4525-Q21 Top Layer Signal Routing of Key Components

#### 3.1 Decoupling Capacitors and Power Supply Connections

##### 3.1.1 Small Value Decoupling Capacitors

With the placement of C16 and C19 directly adjacent to the VP and PGND pins on the top and bottom of the CS4525, the connections are straightforward. **More than one via should be used to connect the VP and GND planes to the cap on each output's power supply pins.** This will reduce the inductance to the internal power planes and help minimize power supply ringing. The vias should be placed outside of the capacitor and not between the CS4525 and capacitor. The location of the vias relative to the capacitor pad will be based on any other nearby components or signal traces.

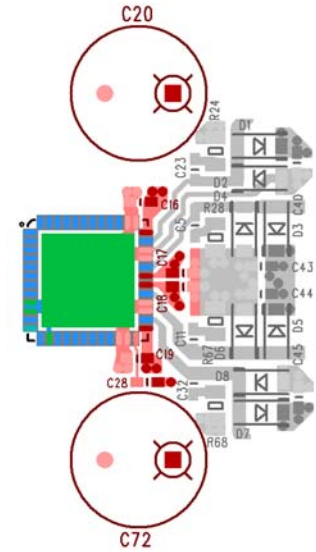
**Both the VP and GND vias should be kept close to the capacitor pads and close to each other in order to minimize the total loop path and EMI.** Do not use a top layer trace to connect the power supply pins to the VP post on the bulk capacitor. This can create a long high frequency return loop and can be more inductive than connecting directly the power supply pins to the layer 3 VP plane close to the capacitor and CS4525.

The CS4525 PGND pins (22, 23, 27, 28, 33, 34, 37, and 38) should also be connected to the grounded thermal pad. These will be the primary GND connections for the center PGND pins and secondary connections for the top and bottom PGND pins.

The C28 ramp capacitor should be connected to pin 24 of the CS4525 with a top layer trace. If C19 is placed and routed properly, this can be accomplished with a straight, 8 mil trace that runs between the pads of C19.

Due to the routing of the OUT1 - OUT4 switching outputs from the CS4525, location requirements of the RC snubber, and location requirements of the Schottky diodes, there is not much available board space remaining for the two center decoupling caps (C17 and C18). [Figure 9](#) and [Figure 10](#) show how placement and routing of these capacitors should be implemented, as on the CRD4525-Q21. Two vias are again used to connect the top layer VP connection to the layer 3 VP plane, and the vias reside outside of the capacitor. **Do not place vias between the center decoupling caps and the VP pins on the CS4525.** After the rest of the routing has been completed and if there is remaining room, the size of the top VP level traces can be increased to further lower the impedance of the VP to CS4525 connection.

The center PGND pins (27, 28, 33, and 34) are connected to the GND through the thermal stitching under the CS4525. To keep the layout small, the GND return of the C17 and C18 decoupling caps will be shared with the snubbers and the protection diodes. This will create a small copper island where all 3 sets of components are connected to GND through multiple vias. This top layer GND island with multiple vias is created in order to keep the backend layout compact.



**Figure 10. Capacitor Routing**

### 3.1.2 Electrolytic Capacitors

**It is recommended that through hole radial electrolytic capacitors are used** if possible. This will allow the best multi-layer GND connection and the shortest decoupling path between the VP and GND layers. Given the stackup, the board's GND connects to the bulk capacitors on layers 1, 2, and 4, as on the CRD4525-Q21.

The CRD4525-Q21 board's VP layer connects to the bulk capacitors on layer 3. If manufacturing processes permit, the thermal relief connecting the through hole to VP layer should be removed. Otherwise, the thermal reliefs on VP should be minimized as much as possible in order to create the lowest impedance path across all frequencies to the bulk capacitors.

Thermal reliefs on the GND layers should be also minimized to create a low impedance path to the bulk capacitors at a broad range of frequencies. It is likely that if the thermal reliefs on all three layers are removed the board will act as too much of a heat sink and may cause assembly issues, so if it is possible to remove the reliefs on only one layer, select layer 2. This will reduce the inductance between the GND plane and the capacitor. Even if the thermal relief on layer 2 is removed, be sure to also minimize the thermal reliefs minimized on layers 1 and 4.

If the board developer is required to use surface mount electrolytic capacitors instead of the recommended through hole capacitors, **make sure to have a solid and redundant connection to VP and GND.** Multiple VP vias to layer 3 and multiple GND vias to layer 2 should be used in order to create as low of an inductive path as possible from the inner layers to the capacitors. Using only 1 or 2 small vias per pad will often reduce the effectiveness of the bulk capacitors, contributing to increased power supply bounce, ripple, and potential EMI issues.

### 3.2 Snubber Layout

The switching output traces will run directly underneath the capacitor pads of the RC snubbers. For purposes of keeping everything compact and to reduce loop area, the entire pad should be completely on top of the OUT1-OUT4 switching outputs. The connection between the capacitor and resistor should be kept as short as possible.

Multiple vias to GND are recommended to minimize the return path inductance. Take note of the 3 via pattern used on the snubber network resistors (R24 and R68) for the CRD4525-Q21. This pattern is used for multiple connections and is a good general purpose via pattern where high frequency signals may be involved.

PCB board manufacturers can have different tolerances and levels of quality. Adding redundancy helps to reduce the effects of board variations. The 3 via pattern keeps the distance from the center of the pad to any of the 3 vias as short as possible without consuming much board area. This allows for close component placement without violating layout keepout or via to part distancing rules.

For the snubber resistors residing on the center landing between the switching output traces (R28 and R67), unless very small vias are used, there is not enough room to use the same 3 via pattern as with R24 and R68. The vias on this top layer center GND island are shared between the decoupling caps, 2 snubbers, and 2 low side protection diodes. The via placement used on the CRD4525-Q21 is shown in Figure 11.

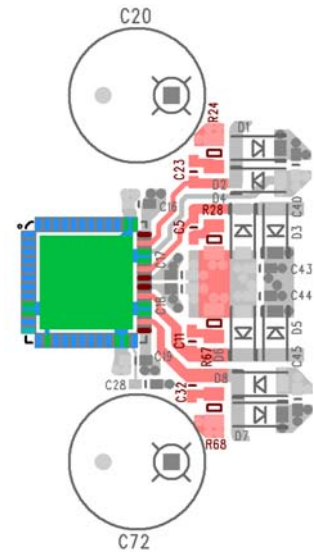


Figure 11. Snubber Layout

### 3.3 Protection Diode Layout

The switching output traces will run directly underneath the Schottky protection diode pads. If using a 40 mil (or wider) trace and a RB160M schottky diode, the entire pad will be able to fit on the output signal trace.

A 3 via pattern, similar to what is used with the two snubber resistors (R24 and R68), should be used for the protection diodes (D1-D8) and diode pair resistors (C40, C43, C44, and C45). Having a solid connection to the internal planes is very important with the Schottky diodes. These diodes can switch on and off very quickly after a rising and falling edge of the CS4525's outputs. They should have a low impedance path to the internal VP and GND planes. If they are connected with only a single via, there is a high risk of increased ringing, increased radiated EMI emissions, and decreased effectiveness of the protection diodes. Figure 12 illustrates how the diodes were connected on the CRD4525-Q21 board.

The diode pairs for OUT1 and OUT4 are rotated 90 degrees. This is due to the location of the inductors (shown in Figure 13) which have been placed to keep the amplifier design small. After OUT1 and OUT4 have passed the snubber circuitry they each make two small, consecutive, 45 degree bends and proceed vertically away from the OUT2 and OUT3 switching output traces. The protection diodes D1, D2, D7, and D8 are connected directly on top of the trace before OUT1 and OUT4 reach the inductors.

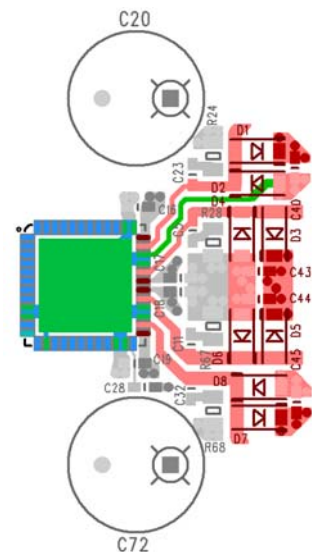


Figure 12. Diode Layout

Between OUT1 and OUT2, there is a 15 mil ground strip connected to pin 34 on the CS4525 and to the GND connection of D2 on the CRD4525-Q21 board. This ground strip is shown in green on Figure 12. Until reaching the protection diodes, OUT1 and OUT 2 are close to each other. The ground strip helps isolate OUT1 and OUT2 from each other and reduce the potential for coupling. The ground strip is optional, but can

be used to help prevent cross talk between the single ended OUT1 / CH1 and OUT2 / CH2 outputs while the traces are close to each other.

The low side protection diodes (D4 and D6) and diode pair capacitors (C43 and C44) on the center landing complete the GND island. The high side protection diodes (D3 and D5) and capacitors should be connected together with a single VP island.

### 3.4 Low Pass LC Filter Layout

The full-bridge switching outputs (OUT3 and OUT4) are run differentially to the Schottky diodes, where OUT4 branches off towards the input of L3. The example in Figure 13 illustrates this with the CRD4525-Q21 board. After the connection to the Schottky diodes, the traces are continued towards the inductor inputs. Since the differential pair has been broken to branch out to the two inductors, make sure to keep the trace lengths similar. Keep in mind that **there is a lot more high-frequency energy on these traces before they reach the inductors** of the LC filter than after they have passed through the inductors. This is an important reason why the component placement, routing and attention to detail are more critical before the inductors than after passing through the inductors of the low pass filter.

The full-bridge output traces will be brought closer to each other again when connecting to the through hole capacitor (C38). Connect to the capacitor in line with the traces. Do not merge the two traces back into a differential pair only to break them again to connect to the capacitor, and do not use a “T” branch or create any stubs to connect to this capacitor. After connecting to the capacitor the OUT3 and OUT4 traces should be rejoined as a differential pair. The differential pair should then be maintained until reaching the output connectors.

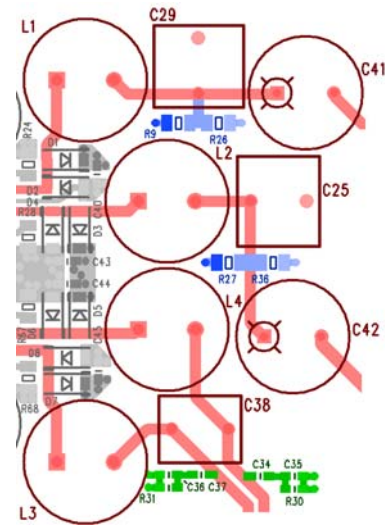


Figure 13. LC Filter and Anti-Peaking Layout

After reaching the high side and low side Schottky diodes, the half-bridge switching output’s path (OUT1) is continued out towards the input of L1. In this example, C29 and C41 are placed so that the signal path coming out of the inductor is essentially a straight line, as shown in Figure 13. This is an ideal output case. It is short, simple, and efficient. However, due to board space requirements, this may not be possible with both half-bridge channels after the inductor. The layout example used for OUT2 is another alternative.

With the routing of OUT2 on the CRD4525-Q21 board, total filter footprint size and the location of the speaker output terminal are taken into account in order to complete the filter. In this example, the signal is routed directly out to C25 and then routed down to C42. This brings the signal closer to the speaker output’s physical location while routing it through the filter components.

For a half-bridge output channel, if it is necessary to route the signals a long distance to the speaker outputs, **do not create unnecessary gaps between components of the LC filter**. Keep the components and routing between them compact. Any long routing traces should be run between the DC blocking capacitors (C25 and C42) and the output connectors.

### 3.5 Anti-Peaking and Pop Suppression Circuit Layout

#### 3.5.1 Full-Bridge Anti-Peaking Circuit Layout

The layout and location of the anti-peaking circuits are not overly critical, and can be moved around based on board sizing requirements. **Keep the circuits relatively close to the output traces after the LC filter and keep the connections between the components short**. The filter pads do not need to reside directly on the output traces as some of the other system components do. However, do not create long con-

nection branches in order to connect the anti-peaking circuits to the output traces, as this can potentially minimize their effectiveness. The orientation of the 2 capacitors and 1 resistor within the circuit are not important as long as the paths between them are kept reasonably short. An example layout of the anti-peaking circuits are highlighted green in [Figure 13](#).

### 3.5.2 Half-Bridge Anti-Pop Circuit Layout

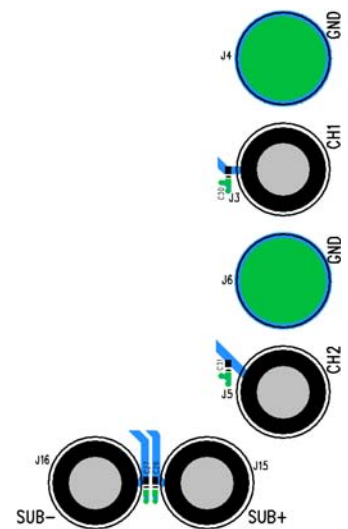
As with the full-bridge anti-peaking circuits, the layout and location of the half-bridge anti-pop circuits are not overly critical. **Keep the resistors close to the output traces between the inductor of the LC filter and the DC blocking capacitor.** They do not need to reside directly on the traces, but make sure to keep any branches relatively short. For example, R9 and R26, in [Figure 13](#), use a short branch to connect the two anti-peaking resistors to the OUT1 signal path. Do not create any branches much longer than this. If room permits, the pads of both anti-pop resistors may be placed directly on the output traces. This is similar to the example used to connect R27 and R36 to OUT2.

## 3.6 EMI Capacitor Layout

The EMI capacitors are placed as a function of the output connectors and not the rest of the filtering. They are put in place to attenuate high frequency energy before it reaches the speaker cables. **The EMI capacitor input side pads should be placed on top of signal paths directly before the output connectors.** Do not create a branch off stub to connect these capacitors, as it will limit their effectiveness.

The EMI capacitor GND side pads can be placed anywhere a solid ground return can be found. Ideally two (or more) vias should be used to connect each EMI capacitor to GND. However, if this is not possible, it is recommended that at least one GND via be adjacent to the pad and at least another one be in the immediate vicinity on the top layer ground fill. Thermal reliefs should be minimized for these capacitors in order to allow for a low impedance return at high frequencies.

[Figure 14](#) shows how the two EMI capacitors for the full-bridge output pair share three GND vias on the CRD4525-Q21 board. In this case the large footprint of the binding post terminals does not leave enough room for two vias per EMI capacitor (C26 and C27). However, there is enough room for two vias adjacent to each of the half-bridge EMI capacitor pads (C30 and C31).



**Figure 14. EMI Capacitor Layout**

## 3.7 Full-Bridge Output Routing

[Figure 15](#) highlights the single full-bridge channel output routing in green and the two half-bridge channels in red. In general, **for both the full-bridge and half-bridge outputs, the signal routing between the CS4525 and the inductors is the most critical section of the layout design.** Before passing through the inductors, the audio signals are square waves, containing much more high frequency energy than after passing through the inductors. The lower frequency audio signals are not reproduced until after the signal passes through the LC filter. The general guidelines of the full-bridge and half-bridge routing are similar with regards to keeping signal paths short and compact until after passing through all of the LC filter components and heading towards the speaker outputs.

With a full-bridge output, the switching outputs of the CS4525 should be routed as differential pairs until they reach the output terminals. There will be times that this will not be possible, such as when connecting to the inductors of the LC filter. However, whenever possible component placement and routing should allow the differential pair to be maintained from the CS4525 to the speaker outputs.

The switching outputs start from the pins of the CS4525 as 15 mil traces. This width is equal to the pad landing for the QFN package used. As the switching output traces move out from the CS4525 they should taper out until reaching a width of at least 40 mils before reaching the snubbers, as in shown in Figure 15. Due to the amount of current flowing through the outputs a minimum of 40 mil traces is required. After expanding the switching output trace's width to 40 mils, do not reduce them back below 40 mils. Avoid sudden 90 degree trace width changes. All 90 degree turns should be composed of two small 45 degree bends.

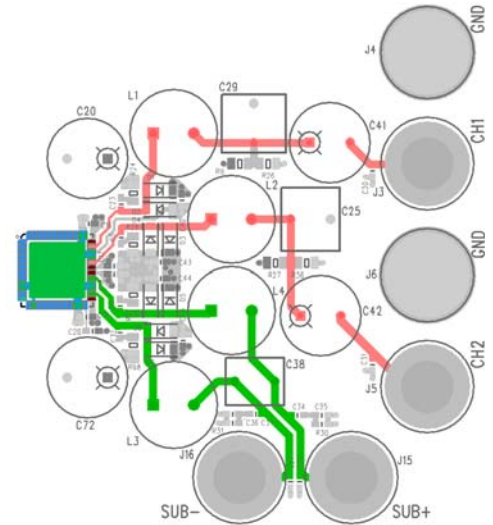


Figure 15. Output Routing

The half-bridge switching outputs are single ended and do not have any differential routing requirements. It is actually better to keep them farther apart from each other to help avoid cross talk. As with the full-bridge outputs, the half-bridge outputs start off as 15 mil traces and taper out to 40 mil traces before reaching the snubbers. The output traces should then be kept a consistent width until reaching the speaker outputs.

### 3.7.1 Half-Bridge Ground Return

It is important that the ground return of the half-bridge speaker output be a solid connection that is low impedance across a broad range of frequencies. In the case of the CRD4525-Q21 boards this has been implemented by keeping the grounds on layers 1, 2, and 4 solid all the way to the binding post terminal. No thermal reliefs are used on any of these layers when connecting to the binding post pads. This reduces any inductance that would be seen on the return path from the half-bridge speaker outputs. If manufacturing processes and the selected speaker connector dictate that thermal reliefs need to be used, keep them as short as possible. This will help reduce the impedance seen by half-bridge return GND connection. Another option would be removing the thermal relief on the internal GND plane (layer 2) only. In a typical board design most of the current will return to the power supply through this layer.

### 3.8 Ground Plane - Layer 2

A solid center ground plane can help prevent multiple performance and EMI issues. It is highly suggested that the center ground plane be at least 1 oz. copper. **The layer 2 GND plane should not split between domains in order to allow for a solid return path.** See [Figure 16](#).

A single, solid ground plane is recommended for best performance. If other components on the system require a split ground plane, this is best implemented on either the top or bottom layer.

When using the recommended stackup, as on the CRD4525-Q21, the layer 2 GND allows for the quickest and lowest impedance return path to the board's input power supply ground. Although, layer 1 and layer 4 typically contain a large amount of ground fill, they should not be used as a primary current return. This is particularly important with the half-bridge speaker output ground return. Layer 2 should be used as the primary current return. The copper ground fill on layer 1 and layer 4 should be connected to layer 2 with via stitching throughout the board, as discussed in [Section 3.10.2](#).

### 3.9 Power Plane - Layer 3

A solid center power plane can also help ensure EMI success. It is suggested that **the power plane (layer 3) be adjacent to the ground plane (layer 2) and be at least 1 oz. copper.**

The power plane(s) should be slightly recessed around the edges from the both ground plane and any ground copper on the top layers. The CRD4525-Q21 board power plane is recessed approximately 80 mils. This will help keep any noise on the power planes from radiating from the outside of the board.

To even further prevent high frequency energy from escaping from the sides of the board, ground stitching with a barrier strip on the power plane can be implemented. An example of a barrier strip can be found on the CRD4525-Q21 board in [Figure 17](#); this is the green ring of ground surrounding the blue and brown power planes. The ground stitching can be found in [Figure 20](#).

With layer 3 being split between VP and VD, it is recommended that simple shapes are used to split the power supply planes. Do not form irregular shapes with the power supply domains. Avoid long narrow branches or fingers to connect components together on the same power plane. Do not try to get too fancy. Keep the power plane layout as simple as possible.

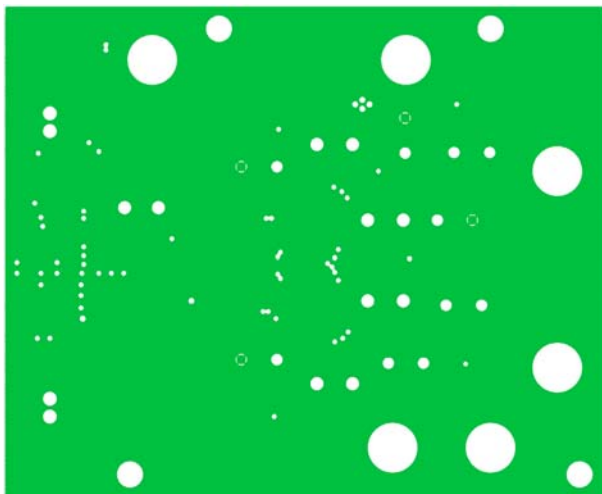


Figure 16. Layer 2 (GND)

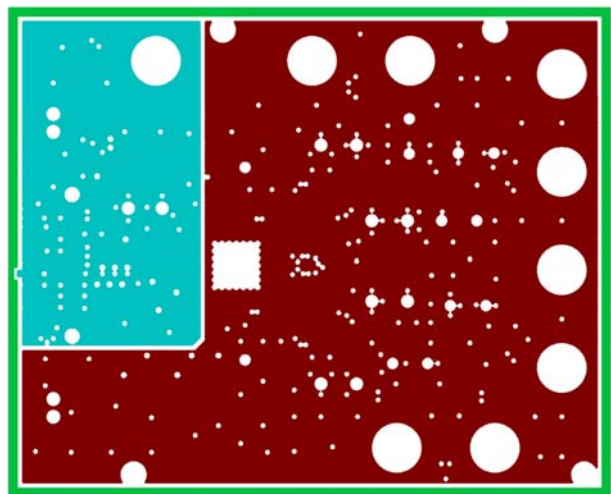


Figure 17. Layer 3 (VD, VP, and GND Ring)

### 3.10 Top and Bottom Signal Layers

Whenever possible, all of the **signal routing in the areas around the CS4525 should reside on the top layer**. All unused areas should be filled with copper and grounded to the layer 2 GND. Make sure there are no floating ground fill islands on the top or bottom layers. **All ground fill should be connected to the layer 2 GND** through multiple via connections. Any power supply ground connections should be made as solid as possible on layers 1, 2, and 4 (when using the same stackup as the CRD4525-Q21).

Figure 18 and Figure 19 contains the copper filled layout of the top and bottom layers of the CRD4525-Q21 board. Note that all of the signals in the vicinity of the CS4525 reside on the top layer. Figure 20 highlights all of the via connections on the CRD4525-Q21 board.

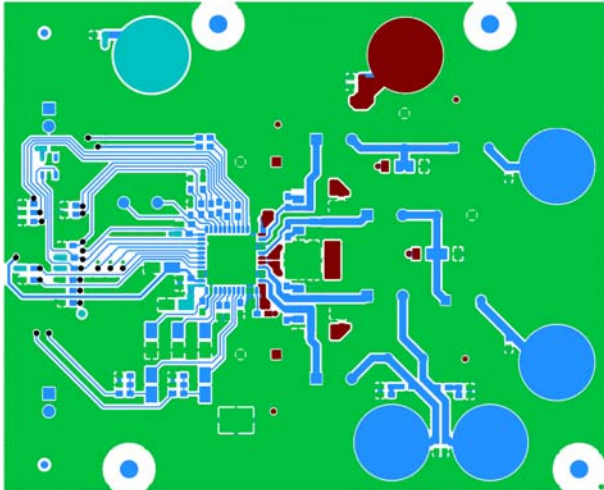


Figure 18. Layer 1 (Top Layer)

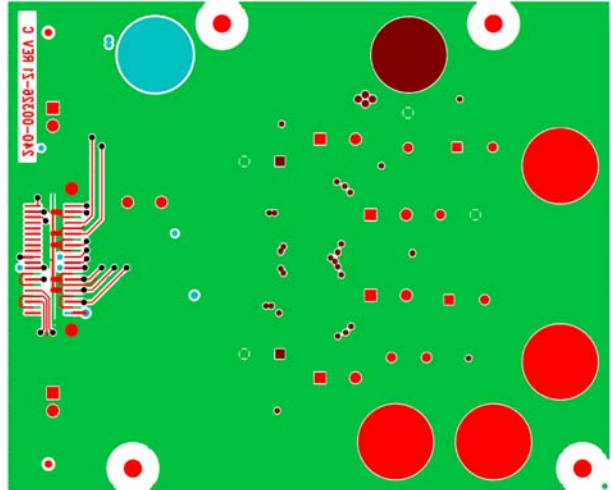


Figure 19. Layer 4 (Bottom Layer)

#### 3.10.1 General Signal Routing Recommendations

It is best to keep the low voltage analog and digital signals on layer 1 whenever possible. Since layer 2 is the GND return layer, this will allow for a return path directly under the original signal. If a low voltage signal is residing on layer 4, it will then be directly on top of one of the power planes.

If it is necessary to route a particular signal from layer 1 to layer 4, **do not cross power domains**. If a signal is a part of the VD power domain, it is best to keep it on top of the VD power plane. If a signal is a part of the VP power domain, it is best to keep it on top of the VP power plane.

### 3.10.2 Ground Stitching

With there being large surface areas of GND on layer 1 and layer 4 there is a need to make sure that all of the grounds are at the same potential across the PCB and across frequency. The most straight forward way of doing this is by **stitching the 3 layers together in multiple locations throughout the board**. Care should be taken not to implement too much GND stitching as it will start to impact the performance of layer 3 (VD and VP).

There are two approaches to implementing via stitching when connecting grounds together. The first is adding vias after the placement and routing are complete. This approach allows for the most flexibility, and was taken for the CRD4525-Q21. This will require some thought as to where vias are placed. The second approach would be to define a via grid that connects layers 1, 2, and 4 before any components are placed or any routing is done. If the layout tool supports it, the vias in the grid will automatically be removed as components are placed and routed. This would help ensure that there is a low impedance path between the 3 layers if setup properly. The easiest approach would be to **implement a grid and then make sure any small ground fill locations are still connected to layer 2** with more than 1 via after signal routing has been completed.

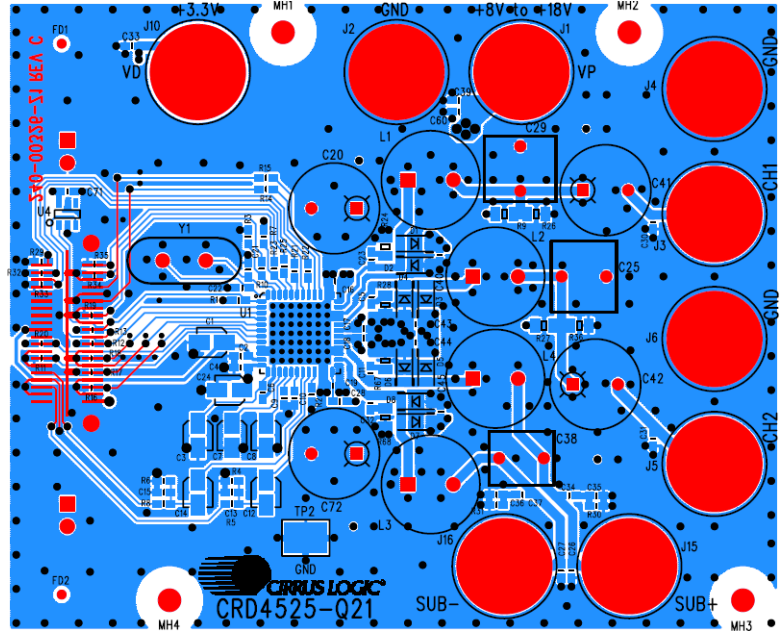


Figure 20. CRD4525-Q21 Component Placement, Routing, and Ground Stitching

Additional **ground stitching should surround the differential speaker outputs**. This will reduce the potential for high frequency energy on the board to radiate off of the board. As with most of the layout, the stitching is more important and has a greater impact between the CS4525 and inductors than between the inductors and the speaker outputs. This is due to high frequency energy being attenuated by the low pass LC filter. Figure 20 illustrates the ground stitching throughout the CRD4525-Q21 board.

### 3.10.3 Thermal Stitching

**Via stitching under the CS4525 is necessary in order to help dissipate thermal energy** produced by the switching output FETs of the Class D amplifier. A majority of the energy dissipated will flow through the board and radiate out from the bottom layer. In order to provide a good thermal conduction path, a grid of solid ground vias should be placed under the CS4525. Do not use vias with thermal reliefs. Figure 20 shows the 7 x 7 via array that is implemented on the CRD4525-Q21.

**Avoid traces on the bottom layer in the vicinity of the CS4525.** Traces in this area will produce thermal resistance and will reduce the ability of the PCB to dissipate thermal energy.

**Refer to AN315 Thermal Considerations for QFN Packaged Circuits** for more information on how via construction and layout can affect thermal performance and suggested methods for thermal stitching for the CS4525.



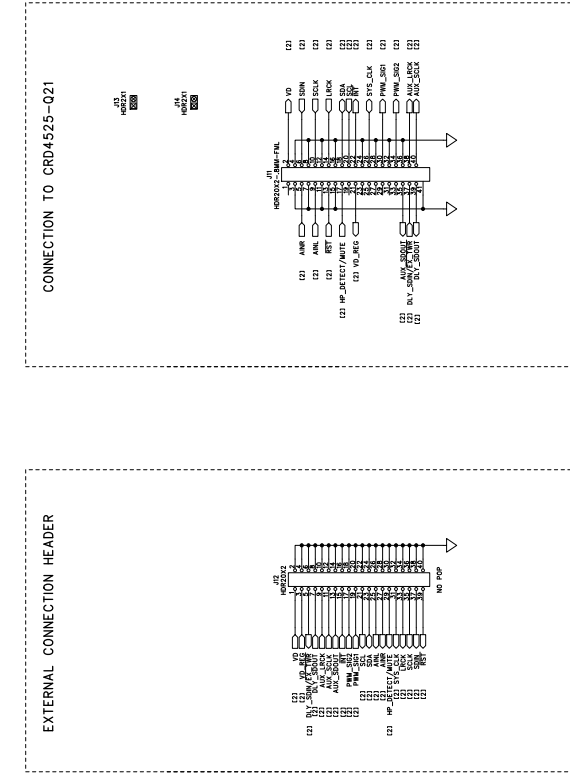


Figure 22. CRD4525-Q21 Breakout Board Schematic

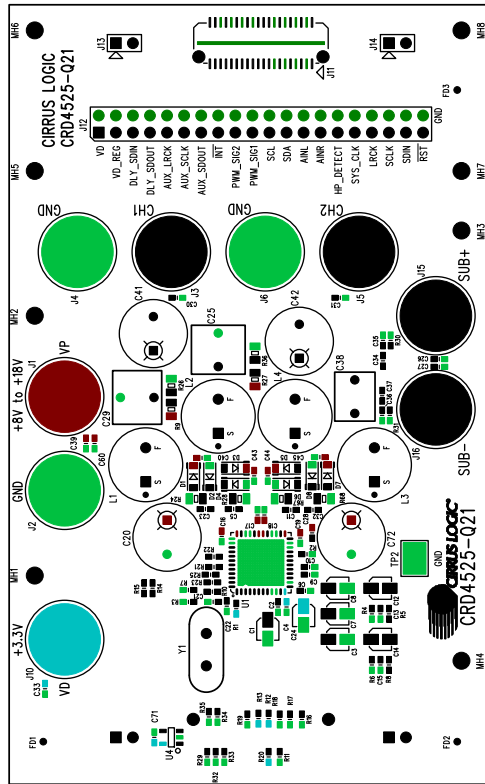


Figure 23. CRD4525-Q21 Board Silkscreen Top

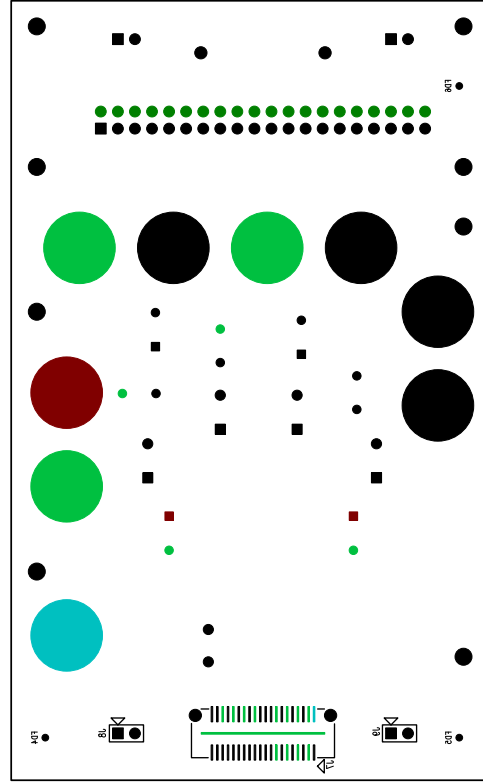


Figure 24. CRD4525-Q21 Board Silkscreen Bottom

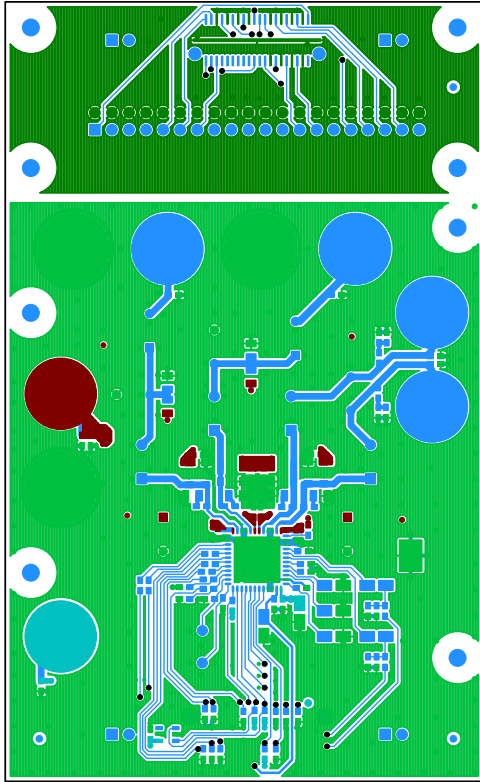


Figure 25. CRD4525-Q21 Layer 1 (Top Side)

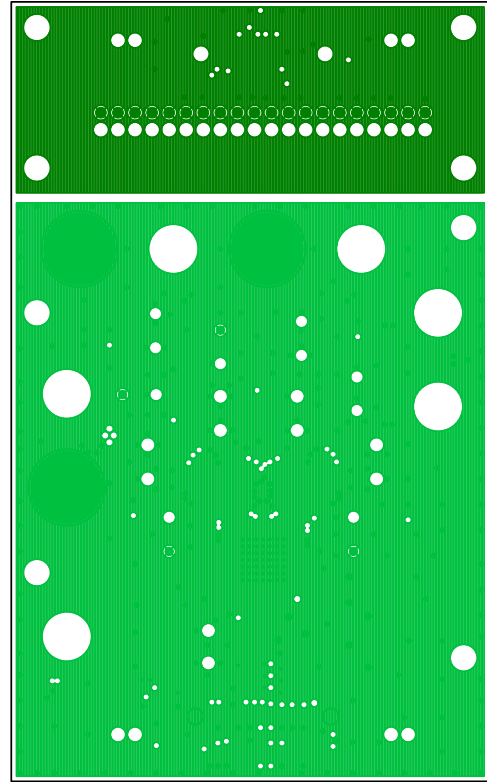


Figure 26. CRD4525-Q21 Layer 2

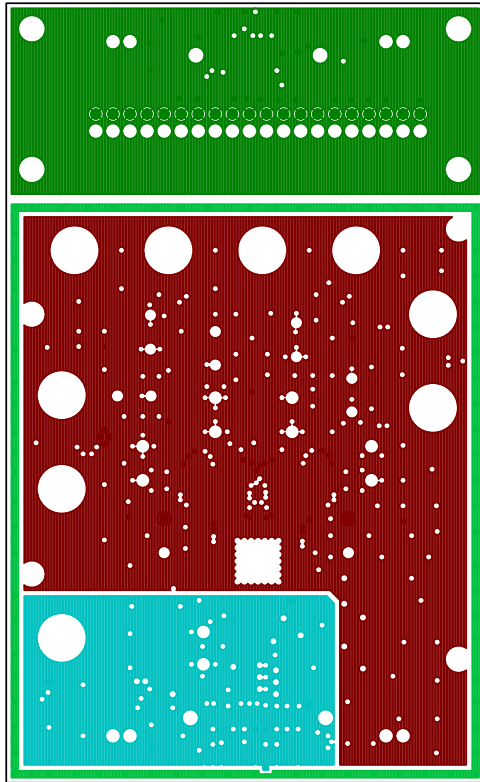


Figure 27. CRD4525-Q21 Layer 3

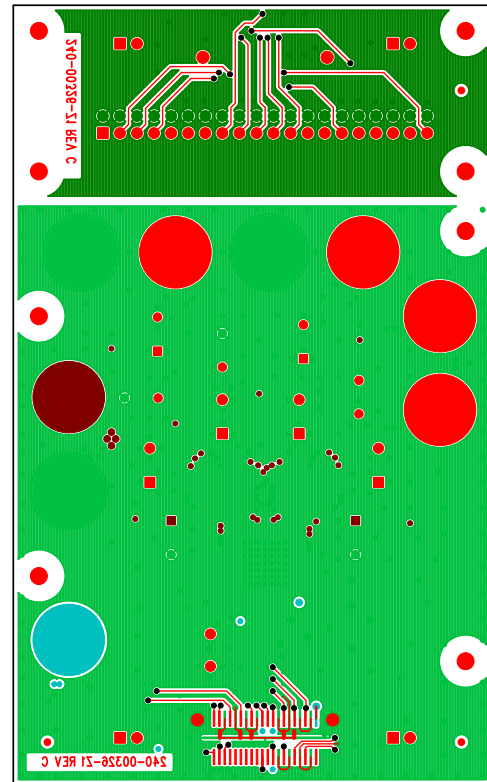


Figure 28. CRD4525-Q21 Layer 4 (Bottom Side)

## 5. REFERENCES

1. Cirrus Logic, Inc. AN315: "Thermal Considerations for QFN Packaged Integrated Circuits".

## 6. REVISION HISTORY

Revision	Changes
REV1	Initial Release

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