# Audio A/D Conversion
# with an Asynchronous Decimation Filter

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## 1. INTRODUCTION

Modern high-performance delta-sigma analog-to-digital (A/D) and digital-to-analog (D/A) audio conversion systems require a high frequency system clock (master clock) for their conversion processes, generally in excess of 12 MHz. Jitter on this clock is a significant source of performance degradation in these systems. This is generally not a problem in products that include the converters as well as a crystal based clock. However, this can be a particularly difficult problem to address in networked audio systems, recording systems which utilize a "house sync" signal and other systems that require long-distance routing of the high frequency clocking signal within the system, such as a mixing console. A common denominator of these systems is that the conversion nodes and the network operate at the same sample rate or within the same clock domain. The most common approach to recover a low-jitter master clock in these systems is to make use of a phase-lock-loop (PLL). PLL circuits take several forms and have their advantages. However, often times the jitter performance is less than desirable or the PLL does not have a sufficient frequency range, especially in voltage controlled crystal oscillator circuits, to cover all of the required sample rates.

An alternative approach is to create a system architecture where the A/D and D/A conversion nodes operate within local clock domains which are independent of the network or system clock domain. A system with independent clock domains can easily be accomplished with the use of a sample rate converter (SRC), as shown in Figure 1. This architecture also allows the conversion processes to operate at a fixed sample rate which is always higher than the network or interface sample rate. The fundamental advantage of this approach is that the conversion processes are immune to interface clock jitter and are controlled by a local jitter-free crystal oscillator.
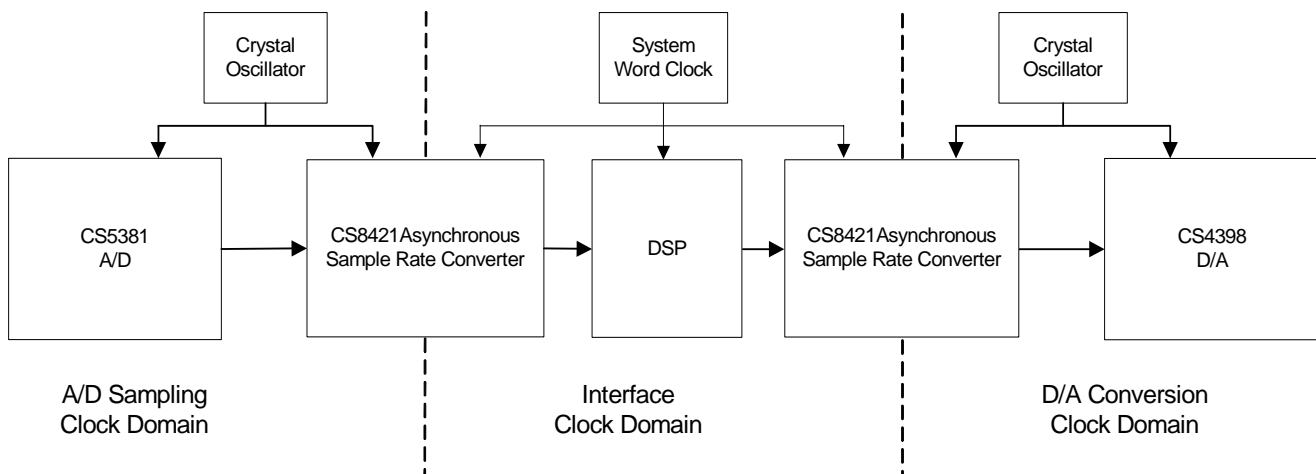


**Figure 1.  Audio System Architecture with Independent Clock Domains**

It is interesting to look at this application from a different perspective. Modern A/D converters utilize digital decimation filters which convert the highly oversampled data to the standard audio sample rates of 44.1, 48, 96 or 192 kHz. These decimation filters perform this function in a synchronous manner where the ratio of the input to output sample rates is fixed, generally either 512, 256 or 128. Essentially, these digital filters downsample the A/D sampled data to a lower sample rate in a synchronous manner. A similar procedure occurs with the digital interpolation filter in the D/A conversion process where the input sample rate is raised to a higher sample rate prior to the digital-to-analog conversion. Consider the fact that in the proposed application the conversion processes can easily be configured such that the A/D and D/A conversions are always operating at a higher sample rate than the interface or network. In this configuration, the SRC is operating as either a decimation or interpolation filter but in an asynchronous manner. Essentially, the integer multiple constraint imposed by standard synchronous decimation and interpolation filters no longer applies. It is this attribute that allows the conversion processes to operate in clock domains which are independent of the network or interface.

In this application, the output of the CS8421 is configured as a slave to the interface system clock. There are several advantages to this approach. The first is the simplicity of changing the system sample rate. Since the conversion process is operating asynchronously from the network, a simple change of the network Left/Right or Word clock is all that is required to change the system sample rate, since the output sample rate of the SRC is determined by the input Word clock. There is no longer a need to reconfigure either the A/D or D/A converters for changes in the system sample rate. The second advantage is that the fact that the output sample rate is dependent on the frequency of the incoming word clock which ensures that the outputs of multiple CS8421 devices are synchronous and phase-matched. The third advantage is that it allows multiple devices to be configured in a Time Division Multiplex (TDM) multi-channel interface.

# 2. ADDITIONAL FEATURES

The inclusion of the CS8421 in the system also adds additional, and valuable, functionality. These unique functions address many of the issues and design challenges associated with networked audio systems and other high-performance multi-channel applications.

- **Selectable Output Data Resolution** - The CS8421 utilizes full 32-bit internal processing and provides the option to output the full 32-bit data word. In addition to the full precision 32-bit data, the device has the functionality to properly dither and truncate the 32-bit data to word lengths of either 24, 20 or 16-bits. The dither between left and right channels is uncorrelated.

- **Support for all Industry Standard Data Formats** - The CS8421 supports all of the industry standard data formats including Left-Justified, Right-Justified and I$^2$S. Figure 2 illustrates a typical multi-channel implementation using these formats.

- **Multi-Channel TDM Interface** - In addition to the standard serial audio interface, multiple CS8421 devices can be configured to implement a multi-channel Time Division Multiplex (TDM) interface. The CS8421 can support a 4-channel TDM at 192 kHz, 8-channels at 96 kHz and 16-channels at 48 kHz sample rates. The block diagram for a 6-channel TDM implementation is shown in Figure 3. Additional channels can easily be added.

- **Greater Digital Stopband rejection over the CS5381** - The digital filter in the CS8421 dominates the filter response in this application. As a result, the minimum stopband rejection is 125 dB.
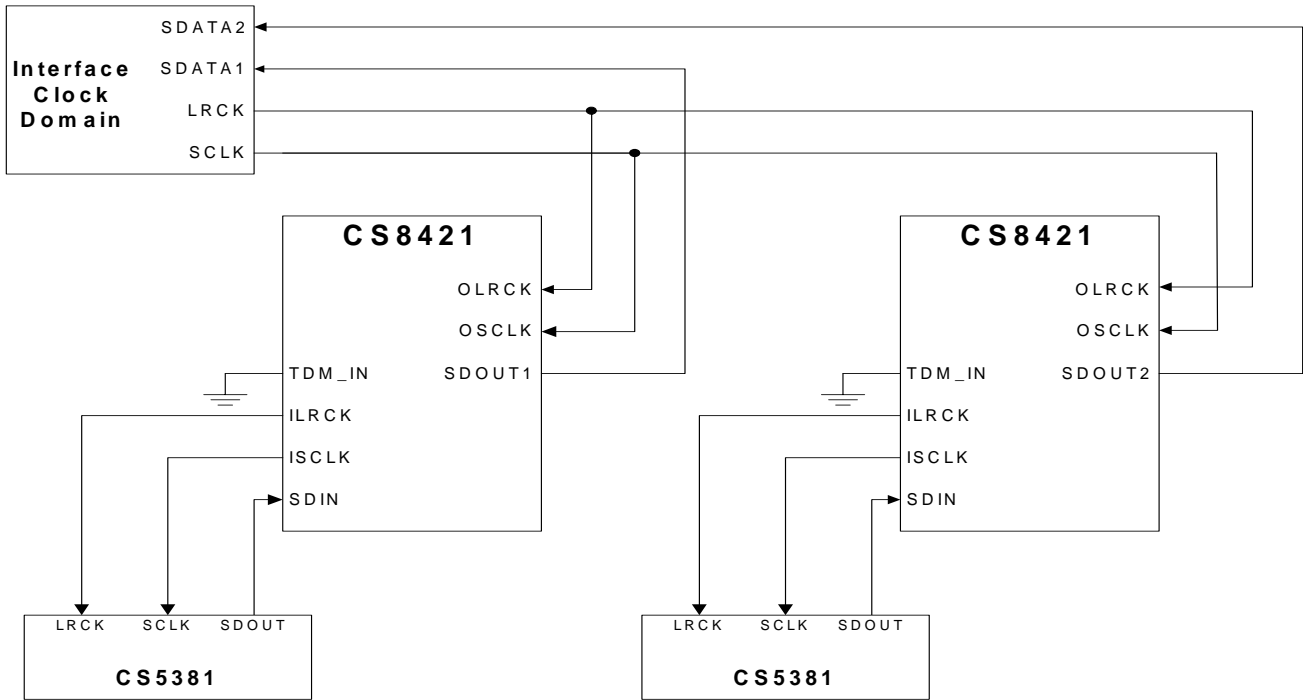
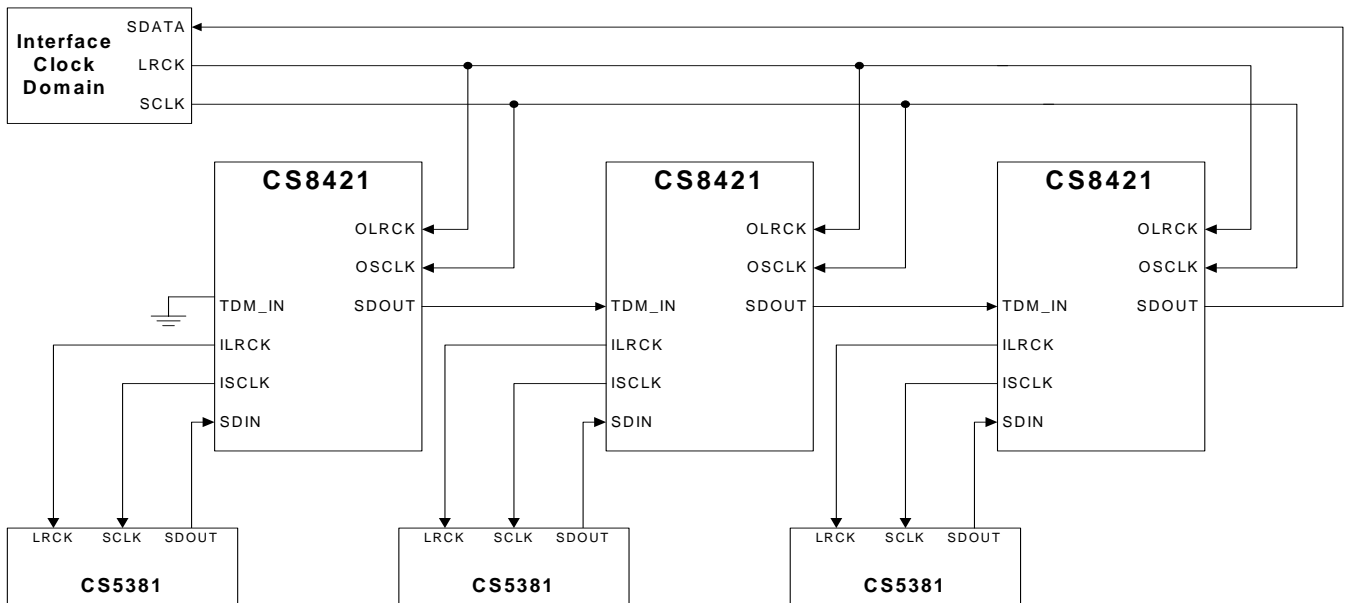**Figure 2. 4-Channel Serial Audio Interface Configuration**



**Figure 3. 6-Channel TDM Configuration**

# 3. CRD5381 OVERVIEW

The CRD5381 is a 4-channel reference design that combines the CS5381 Analog-to-Digital Converter and CS8421 Asynchronous Sample Rate Converter to create an analog-to-digital conversion system as described in this applications note. The CRD5381 is essentially a 2-channel design where the 2-channel block has been replicated to create the 3$^{rd}$ and 4$^{th}$ channels. Each 2-channel section includes the required analog input buffer, the CS5381 A/D converter and the CS8421 Asynchronous Sample Rate converter. The reference design also includes clock generation, status reporting and the required system reset functions. In addition, the dual CS8421 devices can be configured for a 4-channel Time Division Multiplex (TDM) interface.

The intent of the CRD5381 and supporting documentation is to create a design reference that can be considered a "cut and paste" reference to create a multi-channel A/D conversion system. Please also refer to the CS5381 and CS8421 data sheets for specific product information and specifications. These documents are available online at http://www.cirrus.com. The CRD5381 reference design is also available from Cirrus Logic.

The following are the typical performance specifications that can be expected from a CRD5381-based design.

- **Dynamic Range (A-weighted) — 120 dB**

- **Total Harmonic Distortion + Noise — -110 dB**

- **Resolution — 16 to 32 bits**

- **Maximum Downsampling Ratio — 7.5:1**

- **Minimum Stopband Attenuation — 125 dB**

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